KSE | Kyiv School of Economics

School of Engineering

Micro- and Nanoelectronics Programme

Master's Thesis

Wideband Downconversion Mixer

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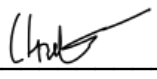
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List of Acronyms

Acronym	Definition
CMOS	Complementary Metal-Oxide-Semiconductor
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
FET	Field effect transistor
IC	Integrated Ciciut
RF	Radio Frequency
LO	Local Oscilator
IF	Intermediate Frequency
NF	Noise Figure
SSB	Single Side Band
DSB	Double Side Band
dB	Decibels
SNR	Signal to Noise Ratio
P1dB	1dB Compression point
IP3	Third Order Intercept Point
IP2	Second Order Intercept Point
HB	Harmonic balance (Large signal analysis)
HBAC	Harmonic balance AC (Small signal analysis)
PSS	Periodic Steady-State analysis
Pnoise	Periodic Noise

Abstract

This project presents the design process and simulation results of wideband downconversion mixer implemented in CMOS technology. The mixer is optimized for maximum conversion gain, while maintaining a wide operational bandwidth in the approximate frequency range of 3–13 GHz.

The transistor-level design and simulations were performed using the Cadence Virtuoso CAD environment. The design is implemented using the open-source SG13G2 PDK with RF-optimized low-voltage transistors. Simulation results demonstrate the performance achievable with the selected technology, topology and design approach.

The proposed mixer architecture provides a foundation for low-power analog circuits intended for SoC-based sensor applications, such as spectrum analysis.

The master's qualification work consists of an introduction, four chapters, conclusions, a list of seven references, and one appendix. The total volume of the work is 49 pages

Acknowledgements

I would first like to express my gratitude to the people at KSE for giving me the opportunity to make this thesis possible.

I am especially grateful to my supervisor, Anton Babushkin, for discussing ideas and providing expert feedback throughout the course of this work.

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Finally, I would like to express my special thanks to Volodymyr Roshchook and Mykola Golub, teachers of the analog design courses, for their patience and explanations during this course.

1. Introduction

1.1 Actuality

The objective of this work is the design of an integrated circuit downconversion mixer implemented in the SG13G2 0.13-µm BiCMOS technology as a key building block of a larger system-on-chip (SoC) project.

The broader goal of the SoC project is to develop a cost-effective solution for radio-frequency spectrum scanning and power measurement integrated within a single chip. The intended application of the proposed system is a fire-detection sensor integrated into a firefighter's protective clothing, capable of alerting the user to the presence of concealed fires behind obstacles such as walls or doors.

A review of existing work indicates that two similar SoC-level solutions have been reported in the publications [1].

Wideband downconversion mixers are widely employed in receiver front ends for applications that require operation over a broad frequency range. Typical use cases include software-defined radios (SDRs), spectrum analyzers, radar warning receivers, aerospace and satellite receivers, automotive and industrial radar system.

1.2 Full project overview

The Spectrum Monitoring Receiver 1 (SMR1) is a research and development project at the Kyiv School of Economics aimed at implementing a wideband spectrum monitoring receiver for detecting and characterizing the power of radio frequency (RF) activity across a broad frequency range 3-13 GHz.

The receiver is intended to be realized as an integrated circuit (IC) — a compact chip solution for spectrum surveillance and signal-presence detection applications. The proposed full project architecture is presented in Figure 1.2.1 [2].

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[1] Wearable Microwave Radiometers for Remote Fire Detection: System-on-Chip (SoC) Design and Proof of the Concept (2)

[2] System top level by Anton Babushkin

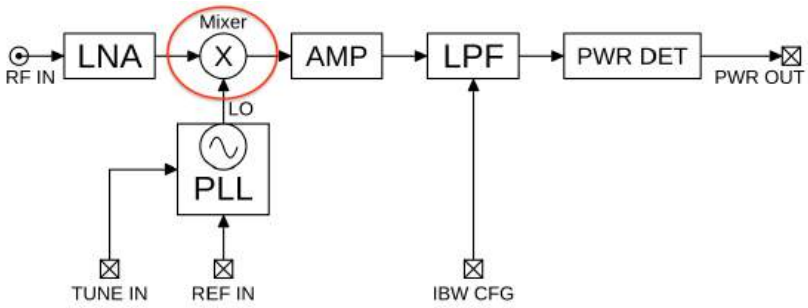


Figure 1.2.1 - IC top level architecture

In this work, the focus is placed on the design of the mixer module. The scope of the work includes the following objectives:

- Definition of a figure of merit (FoM) tailored to the specific requirements of the target application
- Review of best practices and state-of-the-art design approaches for downconversion mixer topologies
- Identification and definition of the key performance parameters of the mixer
- Description of the simulation methodologies used to evaluate these parameters using Cadence SpectreRF
- Analysis of optimization strategies for improving mixer performance.
- Discussion of the fundamental limitations and trade-offs associated with the selected topology and technology.

1.3 Status of current research projects mixers

Comprehensive theoretical foundations and practical design methodologies are presented in standard literature, including Behzad Razavi's *RF Microelectronics*, as well as in numerous publications of the IEEE research community[3]. In this work there references to both of them can be found.

[3] The book source and IEEE researches presented in sources (1) (3) (4) (5) respectively

1.4 Object of research

A downconversion mixer is the primary nonlinear block in a radio-frequency receiver. Its bandwidth directly influences the range of signals that can be processed, making wideband mixer architectures essential for modern multi-standard and broadband applications.

1.5 The importance

As a first step to a bigger SoC project, this work aims to develop a comprehensive understanding of downconversion mixer design and its underlying operating principles, including:

- The operation and application of the Cadence SpectreRF simulation environment
- Key performance metrics of downconversion mixers
- The impact of mixer characteristics on the overall performance of an RF receiver
- The acquisition of design expertise applicable to future RF and analog integrated circuit projects

1.6 The aim of research

This section outlines the objectives and methodological steps of the present work. The study is conducted with the aim of developing a systematic understanding of downconversion mixer design through the following stages:

- Mathematical analysis of the operating principles of downconversion mixers
- Identification of the key performance metrics used to evaluate mixer quality
- Review of the main mixer architectures, including state-of-the-art solutions, along with their advantages and limitations
- Experimental evaluation of the defined performance metrics through transistor-level simulations using Cadence Virtuoso

- Analysis and comparison of the obtained simulation results

1.7 Methods of research

The research presented in this work is based on a combination of analytical, theoretical, and simulation-based methods. These include a systematic review of scientific publications accessed through Google Scholar and IEEE journals, theoretical analysis grounded in the mathematical and physical principles of frequency conversion, and transistor-level experiments and simulations performed using the Cadence Virtuoso and SpectreRF simulation environment.

1.8 Innovations

This work presents one of the first implementations of a downconversion mixer designed using the SG13G2 PDK within the academic environment of Kyiv School of Economics, supported by verified Cadence simulation results.

The study also serves as an experimental evaluation of RF-optimized transistors provided by the SG13G2 PDK. These devices incorporate p-substrate guard rings intended to reduce substrate noise coupling, and their behavior is analyzed in the context of wideband mixer design.

1.9 Approach to this work

This work follows a structured design-oriented approach aimed at the development and evaluation of a wideband downconversion mixer. The approach consists of the following sequential steps:

1. Establishment of a theoretical and mathematical foundation for frequency conversion and mixer operation.
2. Identification of target performance parameters based on system-level requirements.
3. Analysis of commonly used mixer topologies and state-of-the-art architectures relevant to wideband applications.

4. Definition of a figure of merit (FoM) tailored to the objectives of the proposed design.
5. Implementation of the selected topology at the transistor level and performance evaluation through simulations using Cadence Virtuoso and SpectreRF.

2. Analytical Overview

2.1 Theoretical background. Mathematical base.

Frequency conversion operating principles and mathematical model according to Behzad Razavi [4].

Mixer is a 3-port system:

- LO - Local Oscillator
- RF - Radio Frequency
- IF - Intermediate Frequency

A mixer performs signal multiplication in the time domain with mixing of two sine waves signals - RF and LO. Mathematically, it looks like this

$$v_{OUT}(t) = v_{RF}(t) \cdot v_{LO}(t) \tag{2.1.1}$$

Since signals can be represented trigonometrically, it becomes

$$cos(a)cos(b) = \frac{1}{2}[cos(a+b) + cos(a-b)] \tag{2.1.2}$$

We obtain a resulting signal as a sum and a difference of frequencies with half amplitude.

[4] Information accordingly to (1)

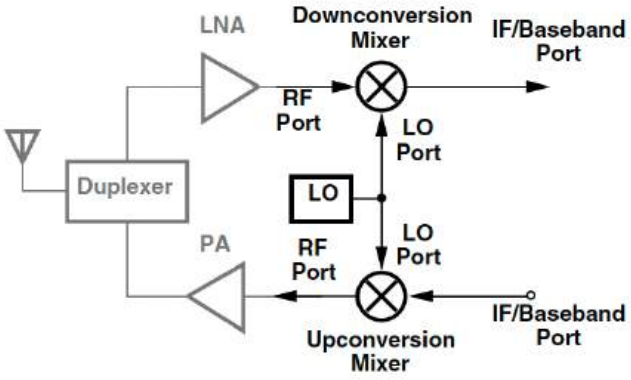


Figure 6.1 *Role of mixers in a generic transceiver.*

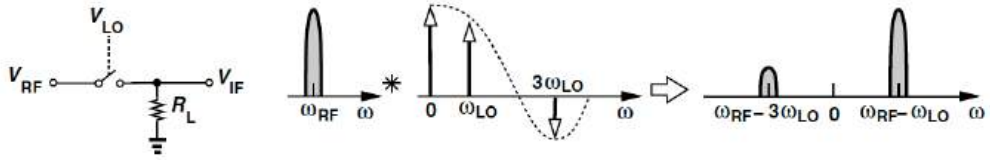


Figure 2.1.1
Top part: demonstrates a hight level architecture of transceiver
Bottom part: RF signal and LO signals multiplication principle visualization

$$v_{OUT}(t) = \frac{A_{RF} \cdot A_{LO}}{2}[cos2\pi(f_{RF)} + f_{LO})t + cos2\pi(f_{RF)} - f_{LO})t] \quad (2.1.3)$$

So we get

$$f_{SUM} = f_{RF} + f_{LO} \text{ and } f_{IF} = |f_{RF} - f_{LO}| \quad (2.1.4)$$

If we use the LO signal as a square wave and multiply the sine wave RF signal by that. Then we can obtain the following mathematical representations.

A square wave LO can be represented as the sum of infinity numbers of odd-numbered sine waves (fundamental harmonic, 3rd, 5th, 7th, etc.), whose amplitudes decrease with their harmonic number. The square wave can be represented in a Fourier Series as:

$$f(t) = \frac{4}{\pi}(sin(f_{LO}t) + \frac{1}{3}(sin(3f_{LO}t) + \frac{1}{5}(sin(5f_{LO}t) + \dots) \quad (2.1.5)$$

And in general terms can be represented as following.

$$v_{LO} = \sum_{n=odd}^{\infty} \frac{4}{\pi n} sin(2\pi n f_{LO} t) \quad (2.1.6)$$

So we get

$$f_{OUT} = |f_{RF} \pm n f_{LO}| (n = 1,3,5,...) \quad (2.1.7)$$

Which means we are generating image frequencies when we have an LO a square form signal, and we have a rich spectral output.

Also, let's put an image here to visualize the circuit and understand what's going on graphically, as shown in Figure 2.1.1 [5].

From the above, we can define the following:

1. LO port working as a switch, that turns on or off, or 1 and 0. The LO signal can be sinusoidal or a square wave.
2. The operation can be viewed as the multiplication of the LO signal with the RF signal.
3. Unwanted harmonics are generated by the nonlinear interaction between the RF signal and the harmonic content of the LO, as well as by RF harmonics and mixer nonlinearities. Also know as mixing spurs.
4. LO port can be defined as non-linear. RF port must remain sufficiently linear to satisfy compression and intermodulation requirements.

From the above, we can define that we are working with a non-linear and time-variant system.

If LO is working as a switch, then we can define the output formula as a function from LO - s(t).

$$v_{OUT}(t) = v_{RF}(t) \cdot s(t) \quad (2.1.8)$$

[5] Figure 2.1.1 and equations 2.1.1 - 2.1.8 is take from (1)

2.2 Performance parameters.

So, let's see how we can work with this system and how to deal with non-linearity.

According to academic publications and Razavi's book, the most important mixer parameters are Noise Figure, Linearity, Gain, and Port-to-Port Feedthrough [6]. We can also see them clearly in all the published mixer designs.

2.2.1 Noise

The mixer introduces additional noise due to device thermal noise, flicker noise, and noise folding mechanisms associated with the mixing process. The noise figure (NF) quantifies the degradation of the signal-to-noise ratio (SNR) introduced by the mixer, by comparing the input SNR to the output SNR. Noise Figure describes a correlation between the SNR at the input (from LNA) and the SNR at the output of the mixer. The mixer usually suffers from the following noise types. The following statements will be discussed in details in the section 2.3 Architectural overview – cover key mixer types and their trade-offs

- Mixers add noise and also fold noise from image frequencies.
- A noiseless unity-gain mixer has a single-sideband (SSB) NF of 3 dB.
- Reason: Image noise folds onto the signal band, doubling the noise.
- Double-sideband (DSB) NF is 3 dB lower than SSB NF.
- Typically, mixer NF in practice is greater than 8 dB.
- Thus, an LNA providing 10–15 dB gain typically precedes the mixer to suppress its noise contribution.

$$NF = \frac{SNR_{IN}}{SNR_{OUT}} \tag{2.2.1}$$

2.2.2 Linearity

Linearity determines how the mixer behaves when exposed to strong or multiple input signals. Linearity describes the extent to which the desired frequency conversion remains proportional when strong or multiple RF signals are present.

[6] Mixer performance analysis from (3) (4) (5)

A nonlinear mixer generates unwanted intermodulation products, harmonics, and spurious tones that interfere with desired signals. We can say that mixers nonlinearity cause to:

- P1dB compression at the output of the mixer
- IP3/IP2 intermodulation distortions at the output of the mixer
- Those nonlinearities cause blocking/desensitization at the level of the receiver.

2.2.3 Conversion gain

Conversion gain measures how effectively the mixer translates input RF power to output IF power. When the input and output are not at the same frequencies. It is defined as and expressed in dB [7].

$$G_C = 10log_{10}\frac{P_{outIF}}{P_{inRF}} \tag{2.2.2}$$

2.2.4 Port-to-Port Feedthrough and Isolation

A mixer is a three-port device (RF, LO, and IF). In an ideal mixer, each port is isolated, and energy does not leak between them.

In practice, parasitic capacitances, device asymmetry, and imperfect switching cause feedthrough and can create undesired distortions to the signals. Such as:

- LO → RF feedthrough
- LO → IF leakage
- RF → IF leakage
- IF → RF back-injection

Those feedthrough effects can depend on a mixer architecture, which will be overviewed in the next section.

[7] Equations 2.2.1 - 2.2.2 are taken from (1)

Poor isolation can lead to difficulty in filtering or extracting the desired IF signal. From the above, we can conclude that Mixer is a non-linear system that suffers from noise, feedthrough effects, and needs some conversion gain, and we need to find a balance between noise, linearity, and gain.

2.3 Architectural overview – cover key mixer types and their trade-offs

Main receiver architectures and mixer topologies overview.

1. Single-sideband (SSB) and Double-sideband (DSB) receivers' architecture
2. Double-balanced vs. single-balanced topologies and their performance parameters.
3. LO waveform - here considered as a part of mixers topologies
4. Active and Passive mixers operating principles and their differences

2.3.1 Single-sideband (SSB) and Double-sideband (DSB) topologies and their tradeoffs.

Single-Sideband (SSB)

is an operation refers to frequency translation in which only one spectral sideband is preserved - upper or lower, while one of them suppressed. This approach improves spectral efficiency and reduces noise contributions from unwanted frequency components.

- In direct-conversion mixers, only noise from the signal band is translated
- Input and output SNR remain equal for a noiseless mixer
- Thus, the SSB noise figure is 0 dB.

Double-Sideband (DSB)

In opposite to SSB, DSB receiver architecture has both upper and lower sidebands in the output specter. This architectures common characteristics are

- Thermal noise in both - signal band and image bands.

- After down-conversion, noise from both bands (signal + image 3ωLO) folds into IF.
- Output SNR becomes half the input SNR (if noise powers are equal).
- Thus, the noise figure for a noiseless mixer (DSB) is 3 dB.

The difference in noise figure between DSB and SSB operation is fundamentally determined by noise folding from multiple sidebands.

2.3.2 Double-balanced vs. single-balanced mixers topologies and their tradeoffs.

A single-balanced mixer is typically driven by differential LO waveforms while employing a single-ended RF input. Compared to mixers driven by a single-ended LO signal, this topology provides approximately twice the conversion gain due to the differential signals at the output. The single-balanced mixer produces differential output signals and, when properly symmetric, suppresses LO–RF feedthrough. However, since only one port is balanced, the topology still exhibits significant LO–IF feedthrough and limited suppression of even-order distortion products.

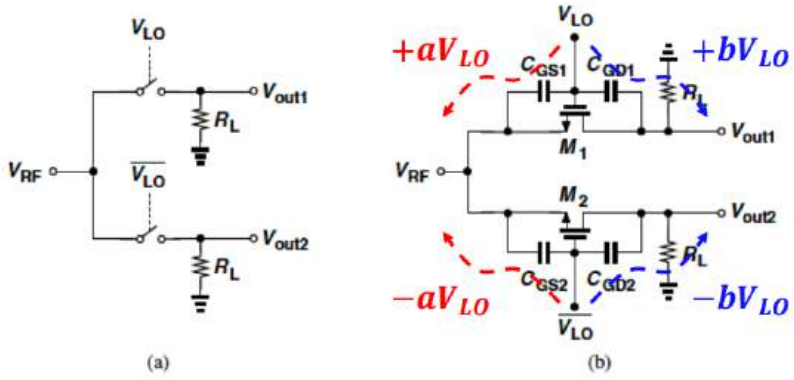


Figure 2.3.1 - Single-balanced passive mixer
LO to RF and IF feedthrough

As we can see, the feedthroughs +aVlo and -aVlo are with opposite sine, so with the good symmetry of the keys, those effects will be annihilated, and Vrf won't suffer. Also, we have the differential signal at the end.

So we can calculate that as

$$v_{O1} = v_{O1} + (b \cdot v_{LO}),\ v_{O2} = v_{O2} - (b \cdot v_{LO}) \quad (2.3.2)$$

$$v_{diff} = v_{O1} - v_{O1}(2b \cdot v_{LO}) \quad (2.3.3)$$

But this topology still suffers from LO-to-IF feedthroughs because they are not cancelling out [8].

Double-Balanced Mixer

Although both single-balanced and double-balanced mixers provide differential outputs, only the double-balanced topology ensures LO-to-IF feedthrough suppression. This is achieved because the LO signal appears with equal amplitude and opposite polarity in the two mixer branches, resulting in cancellation at the differential IF output.

- Two single-balanced mixers are arranged for LO–IF feedthrough cancellation.
- Differential LO and RF inputs; provides high isolation and balanced outputs.
- Output signals preserved; LO leakage signals cancel each other as shown at Figure 2.3.2.
- Can operate with single-ended RF input, but at the cost of higher input-referred noise.

[8] Figure 2.3.1, equations 2.3.1 - 2.3.3 is taken from (1)

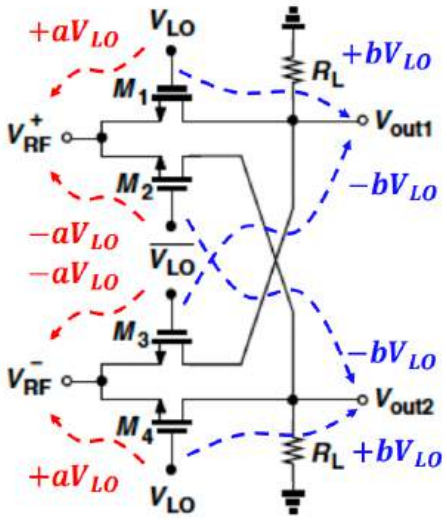


Figure 2.3.2 - Double balanced passive mixer feedthroughs effects

2.3.3 LO waveform

LO Characteristics

Ideally, the LO waveform should be a square wave.

- Ensures abrupt switching and maximum conversion gain.

Impact of Gradual LO Waveform

- Gradual (sinusoidal-like) LO causes overlapping conduction.
- During overlap time (ΔT), all switches are simultaneously ON.
- VRF becomes a common-mode component, producing no useful differential output (signal is “wasted”).
- Gradual switching edges may also raise the noise figure.

Practical Considerations

- At very high frequencies, LO inevitably becomes sinusoidal.
- To minimize overlap, use a large amplitude LO to achieve a high slew rate[9]

[9] Figure 2.3.3 is taken from (1)

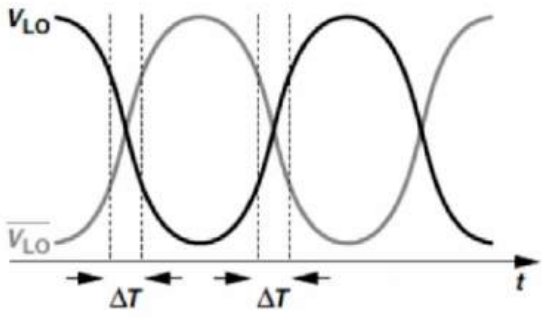


Figure 2.3.3

2.3.4 Active and Passive Mixers

Passive Mixers

Main principles of work:

- utilize transistors as switches - RF signal injected directly to the source of the key.
- Has a resistive or capacitive load
- Switch on the resistance, reduce the gain
- No power consumption, or a small bias to the LO key.
- Provides differential output, which doubles the conversion gain.

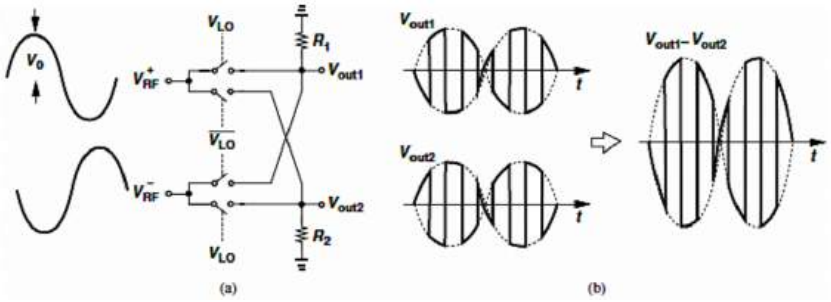


Figure 2.3.5 - Double balanced passive mixer

Switching mixers operate with LO driving MOS transistors deeply into the triode region. Switching mixers achieve high linearity because the MOS devices

operate with very small VDS in the triode region. Conversion gain is calculated for a resistive load, and this mixer is characterized as a Return to Zero mixer.

$$\frac{2}{\pi} = -4dB \tag{2.3.4}$$

If we put the capacitors into a load, we can achieve a Sample and Hold circuit, and a conversion gain can be achieved higher, around 1.48 dB accordingly to the literature[10].

Active mixers

Active mixers achieve conversion gain within one stage.

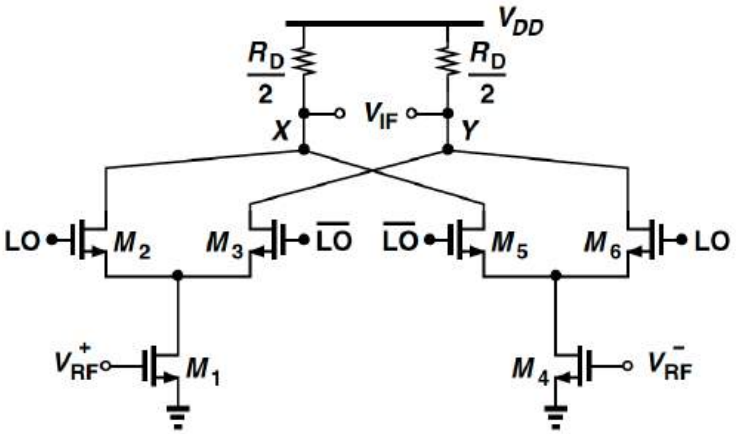


Figure 2.3.6
Double balanced active mixer (Gilber Cell).

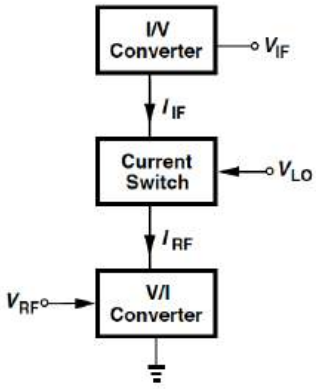


Figure 2.3.7
Operating Principle

Perform three functions simultaneously as seen from the Figure 2.3.7:

- Voltage-to-current (V/I) conversion at input.
- Current steering (commutation) using LO switching.
- Current-to-voltage (I/V) conversion at output. Provide gain due to input transconductance and output trans-resistance.

[10] Figures 2.3.5 - 2.3.7, Equations 2.3.4 - 2.3.6 are taken from (1)

Constructed from two single-balanced mixers as seen from the Figure 2.3.6.

- Rejects LO amplitude noise and enhances linearity.
- Provides differential input and output signals.
- Uses switching quad transistors (M2, M3, M5, M6).

Transistors should operate in the region of saturation and strong inversion for the transconductance stage differential pair transistors. And the LO switching pair should be in saturation to provide perfect current steering. The LO switching pair operating will be discussed in details further in this work.

For the transconductance stage, we need to have linear transconductance and controllable gain. This can be achieved when transistors operate in a saturation region with a strong inversion, with the following proofs.

The conversion gain of this mixer is defined as
RF_IN converted to current by transistor M1:

$$I_{RF}(t) = g_{m1} v_{RF}(t) \tag{2.3.5}$$

Current switching operation by LO transistors M2, M3 should also work in the saturation region to completely steer current from the transconductance stage. LO switching represented by a square wave with fundamental harmonic amplitude

Voltage conversion gain is defined as

$$A_v = \frac{2}{\pi} g_{m1} R_D \tag{2.3.6}$$

Conclusion for the active mixer can be next: we can achieve a higher conversion gain while using a transconductance stage. But this will lead us to less linearity and more noise.

Based on the above information, we can create a comparison table with the main parameters of the mixer, which can guide us through the future choice of the topology. It collected the best-case scenarios for DSB receiver architecture and

mixers with double-balanced topologies. A passive mixer is considered to be with a capacitive load, and an active mixer with a resistive load. We also assume using a 50% LO squared wave duty cycle.

Based on the above, we can create a table with the pros and cons of performance parameters to use different mixer topologies and their main operating principles.

Parameter	**Passive Mixer**	**Active Mixer**	
Noise Figure	2–8 dB (best ≈ 3 dB SSB limit)	5.5–10 dB	Passive mixers approach the fundamental 3 dB SSB limit. Active mixers add gm noise.
Conversion Gain	–3 to +2 dB (C-load, differential ≈ +2.1 dB max)	+5 to +12 dB	Active mixers provide real gain via gm. Passive mixers have insertion loss unless differential.
Port-to-Port isolation	Excellent (40–60 dB)	Good (20–40 dB)	
1dB Compression point	High (+5 to +15 dBm	Low–Medium (–10 to 0 dBm)	Passive mixers can handle large RF signals due to no active device saturation.
IP3	High (+10 to +25 dBm)	Low–Medium (0 to +10 dBm)	Passive mixers are almost linear in RF path → excellent IIP3.
IP2	Very High (40–80 dBm, depends on symmetry)	Low–Medium	Active mixers often suffer from gm mismatch generating IM2.

LO power swing	High (0.5–1.2 Vpp at gate to fully switch Ron)	Low (100–300 mVpp sinus or square)	Passive: large LO drive is needed to push MOS into triode. Active: LO only needs to steer current.
Power consumption	0 mW (gate-driven only)	>2–10 mW typical	Active mixers require DC current (tail current) + Vdd supply.

Table 2.3.1 - Comparison for Active and Passive double balanced mixers

3. Theoretical Part and Hand Calculations

3.1 Different Architectures overview and State-of-the-Art Practical Implementations

In this section 3 published projects with similar technological process of 0.13 μm and wide bandwidth operating performance will be presented with the short overview of each.

3.1.1 A 9-50-GHz Gilbert-cell down-conversion mixer in 0.13-μm CMOS technology

A broadband microwave/millimeter-wave (MMW) Gilbert-cell mixer using standard 1P8M 0.13-μm complementary metal oxide semiconductor (CMOS) technology is presented in this letter. Two radio frequency (RF) transformer baluns are used in the RF and local oscillator (LO) ports to convert single-ended signals to differential signals. Thin-film microstrip line is employed for the matching networks and transformer design. This mixer has a conversion gain of better than 5dB from 9 to 50GHz. Between 5 and 50GHz, the RF- and LO-to-intermediate frequency (IF) isolations are better than 40dB. The RF-to-LO and LO-to-RF isolations are all better than 20dB. The measured noise figure at RF of 15 GHz is

16.4 dB. The high noise figure may be possibly due to the RF-transformer, which has 3-dB more loss than the ideal transformer [11]. No Noise figure reported.

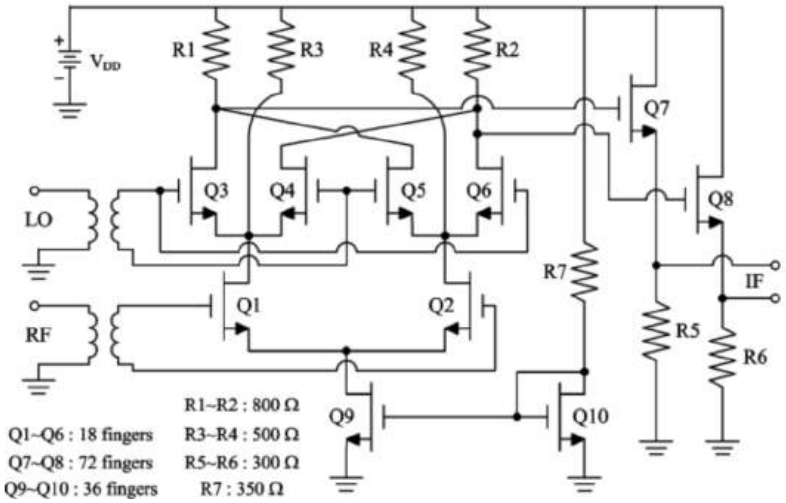


Figure 3.1.1 - Circuit schematic of the double balanced Gilbert-cell mixer, consisting of a Gilbert-cell core, two RF transformers, and two common-drain buffer stages.

3.1.2 A 10–35 GHz Low Power Bulk-DrivenMixer Using 0.13 µm CMOS Process

10-35 GHz doubly balanced mixer using a 0.13-mum CMOS foundry process is presented in this letter. Using the bulk-driven topology, the number of transistors of the doubly balanced mixer is reduced; thus the mixer can achieve a low supply voltage and low power consumption. This bulk-driven mixer exhibits a measured conversion gain of -1 plusmn 2 dB from 10 to 35 GHz of radio frequency (RF) with a fixed intermediate frequency (IF) of 100 MHz. The measured local oscillation (LO) to IF and RF-IF isolations are better than 30 dB. The chip area of the mixer is 0.6 times 0.4 mm2. The total power consumption included output buffer is only 6 mW [12].

No noise figure reported.

[11] Figure 3.1.1 and text is taken from (5)

[12] Figure 3.2.1 and text is taken from (4)

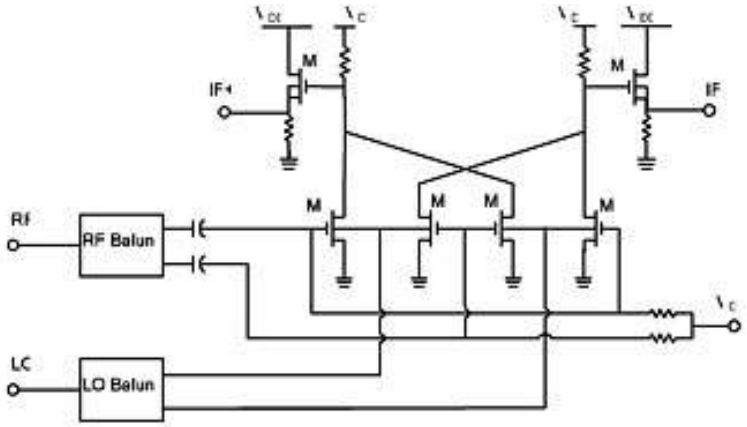


Figure 3.1.2 - Bulk Driven Down conversion mixer

3.1.3 Comparative study of different types of mixer topologies

Department of Electronics and Communication Engineering, Institute of Engineering and Technology, GLA University, India, studied different mixers topologies and presented in this publication [13]. They studied different mixer topologies, and this paper has been presented in SchematicScholar website.

Techniques	Multi-Tanh	Current Bleeding	Folded cascode	Bulk-driven	CCPD	MGTR	Switched biasing
Linearity	High	High	Moderate	Low	High	Moderate	Low
Noise figure	Moderate	High	High	High	Moderate	Moderate	Low
Conversion gain	Low	Moderate	Moderate	Moderate	Moderate	Low	Moderate
Power consumption	High	High	Low	Low	High	High	High

Figure 3.1.3

3.2 Chosen approaches and instruments to resolve the task

3.2.1 Topology

Let's start with the proven topology that is widely used all over the circuits. From the above research, we see that this topology can be used to provide wide bandwidth operating and can be used as a low-power circuit with our low-voltage devices. We can say it is state-of-the-art in mixer design.

[13] Figure 3.1.3 and text is taken from (2)

A double-balanced mixer operates with a differential LO as well as a differential RF signal, as shown. A single-balanced mixer is simple in design and provides moderate gain and low noise figure, but has poor port-to-port isolation between LO to RF and LO to IF, and possesses a low third-order input intercept point (IIP3). A double-balanced mixer provides high port-to-port isolation and has output spurious product rejection capability, according to this research[14]

In mixer design, the double-balanced Gilbert cell mixer is preferred as a core of many mixers due to its benefits, such as higher linearity, low even-order distortion, and good port-to-port isolation. The basic double-balanced CMOS Gilbert cell mixer consists of three stacked stages, i.e., trans-conductance stage, LO switching stage, and output load stage.

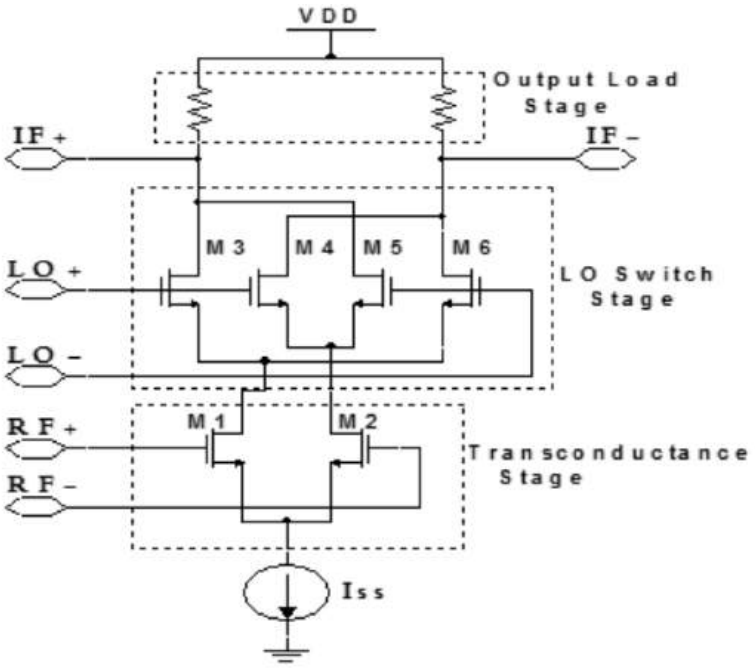


Figure 3.2.1 Schematic of conventional double balanced CMOS Gilbert cell mixer

3.2.2 Instruments, methods, and approaches

The following instruments will be used to complete this task.

[14] A Comparative Study Of Different Types Of Mixer Topologies https://pdfs.semanticscholar.org/a67d/f3b21a461f712145bb40a6e35c4b36b65263.pdf

1. Understand the Figure of Merit and do hand calculations
2. Cadence Virtuoso - to design a schematic
3. Perform DC and Tran analysis to see the operating points and time domain circuit behavior.
4. Optimize calculations.
5. Cadence Spectre RF to perform the simulations like HB, HBAC, PAC, PNOISE
6. Optimize design.

3.3 Hand calculations

In this work we consider the following aspects as the design constrains considered:

1. Operating bandwidth of the Gilbert cell topology with the SG13G2 PDK using RF transistors and RF capacitors.
2. What IF frequency bandwidth we need to achieve?
3. What will be the performance parameters
4. How do we correctly simulate mixer design with Cadence.
5. How can we improve mixer performance

So, let's define design constraints and do the hand calculations.

Conversion gain	> 10dB
RF signal power	-30dBm after the LNA
Noise figure	10dB
IF bandwidth	1-100MHz
RF bandwidth	3-13GHz
Supply Voltage	1.5V

Table 3.3.1 - Design Constrains

Based on the above overview, let's define the design steps and figure of merit of our Gilbert Cell mixer.

The approach to hand calculations can be as following.

- Selection of the transistors
- Gain
- DC Biasing
- Noise Figure

For the Gilbert cell mixer, diffpair transistors should work in saturation, and LO transistors should work as a current steering.

VDD	1.5V
I_{tail}	1.5mA
R_L	1k Ohms
LO swing (peak)	400mV
Channel width RF transistors	20um
Channel with LO transistors	40um
Channel length	0.13um
Vov RF	150mV
Vov LO	100mV

Tabe 3.3.2 - Input parameters

Gain

Let's calculate V_{out} . This will be our DC point on output node. And let's see if we have enough headroom for the amplified signal swing.

$$V_{out,DC} = I_{brach} \cdot R_L = 0.75V \tag{3.3.1}$$

Let's calculate gain and gm first. Since we know the drain current and it is equal to the drain current of the RF transistors, we can calculate gm as, without taking into consideration W, because our drain is set by Itail.

$$gm_1 = \frac{2I_D}{V_{ov}} = \frac{1.5mA}{0.2V} = 7.5ms \tag{3.3.2}$$

And we can calculate the conversion gain as

$$A_v = \frac{2}{\pi} g_{m1} R_D \approx 4.78 \approx 13.68dB \tag{3.3.3}$$

DC Biasing

We can calculate headroom as

$$V_{headroom} = V_{DD} - V_{DS1,sat} - V_{DS2,sat} - V_{out,DC}$$

Where

$V_{DS1,sat}$ - saturation voltage of the RF transistor

$V_{DS2,sat}$ - saturation voltage of the LO transistor.

We assume that for transistors in saturation $V_{DS,sat} = V_{ov}$

So, we can approximate our headroom as.

$$V_{headroom} = 1.5V - 0.75V - 0.1V - 0.15V = 0.5V$$

The saturation voltage of the RF transistor is known and it is 150mV. So Saturation voltage of LO when it is ON is 100mV. ON conditions will be as follows, and this gives us common mode biasing.

$$V_{RF,bias,min} = Vov + Vth = 550mV$$

$$V_{LO,bias,min} = 100mv + Vth = 500mV = V_{LO,on}$$

$$V_{peak,LO} = 400mV$$

$$V_{LO,on} = Vov + V_{peak,LO}/2 = 100mV + 250mV = 350mV$$

This will lower our headroom to -250mV, so we left at 250mV headroom.

$$V_{LO,off} = Vov - V_{peak,LO}/2 = 100mV - 250mV = 350mV = -150mV$$

Capacitors C1 and C2 have a value of 0.3pF to suppress the LO component at the output (which will otherwise help to compress the mixer at the output).

Noise figure

To compute the noise figure due to thermal noise, we first estimate the input-referred noise voltage as

$$V_{n,in}^2 = \pi^2 kT(\frac{\lambda}{gm} + \frac{2}{gm^2 R_D}) = 3.62 \cdot 10^{-}18V^2/Hz \quad (3.3.4)$$

Where λ is 1. We compute the noise figure as a single sideband.

$$NF_{SSB} = 1 + (\frac{V_{n,in}^2}{4kTR_{Rs}}) = 8.5dB \quad (3.3.5)$$

So the hand calculations results goes as following.

Parameter	**Value**
gm (transconductance)	7.5ms
Rl (load resistance)	1k Ohms
Id (drain current)	0.75mA
Av (gain)	13.6dB
NF (Noise figure)	8.5dB
Headroom we have	0.25V
Voltage gain	63mV pp
Rf power	-30dBm
W/W Ratio	1/2
LO power	500mV

Table 3.3.1 - Hand calculations

4. Simulation and Validation.

So we need to understand how these systems behave and how it performs. The next steps should be taken:

1. DC simulation - to see the operating points and if the transistors works accordingly to our calculations.
2. Tran analysis - to see how the signals are changing in time.
3. LO power sweep vs Conversion Gain sweep - to see the optimal LO power signal.
4. Harmonic Balance analysis - to understand Port-to-Port leak edges and Conversion gain from to 1-100MHz IF frequency. We will perform this for corners and in the middle of our mixer range 3-13GHz.
5. PSS + Pnoise - to understand our Noise figure and to see how much noise our system produces.
6. Linearity - 1dB Compression point, IP3, IP2.

4.1 Design and simulations

4.1.1 Design choices

Transistors: rfnmos (Low voltage). Vth = 0.4V. with ptap surrounding ring, Provides a low-impedance return path for substrate currents, so the devices don't affect each other. Guard rings more effectively isolate devices from each other by creating a low resistance ring in the well/substrate around the group. This prevents charge buildup by other devices or fluctuating potential of other devices from affecting the operation of the guarded group, according to the Cadence blog.
For RF purposes, you should use l = [0.13:1.0]um and w = [1:6]um (per single gate). As explained in the technology documents.

Low-voltage RF transistors give higher gm, higher speed, lower noise, and cleaner switching.

Low-voltage transistors have also been chosen due to the low supply voltage we have 1.5V.

4.1.2 Schematic

We start with a classic Gilbert cell mixer, a double-balanced mixer, and simulate its performance. Also, we use RC load to achieve better gain and first-order filtering.

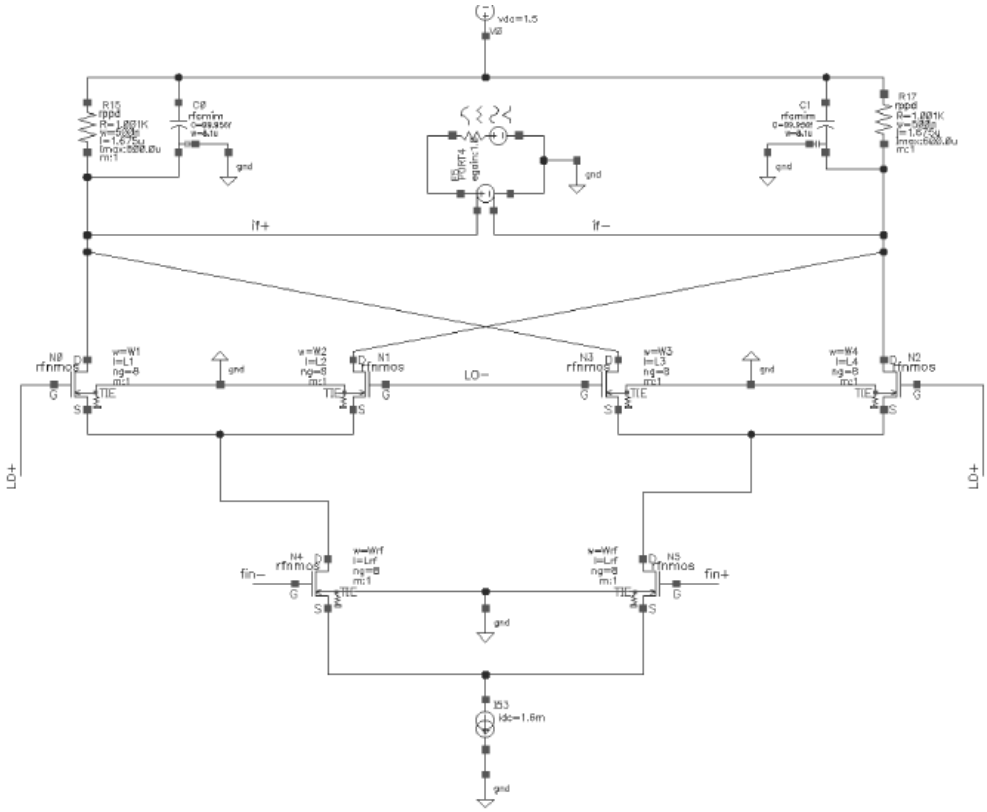


Figure 4.1.1 - Schematic

4.1.3 Test bench set up

We set the ports as follows. The output impedance of this scheme is 0 Ohms, so this is working as an ideal voltage source.

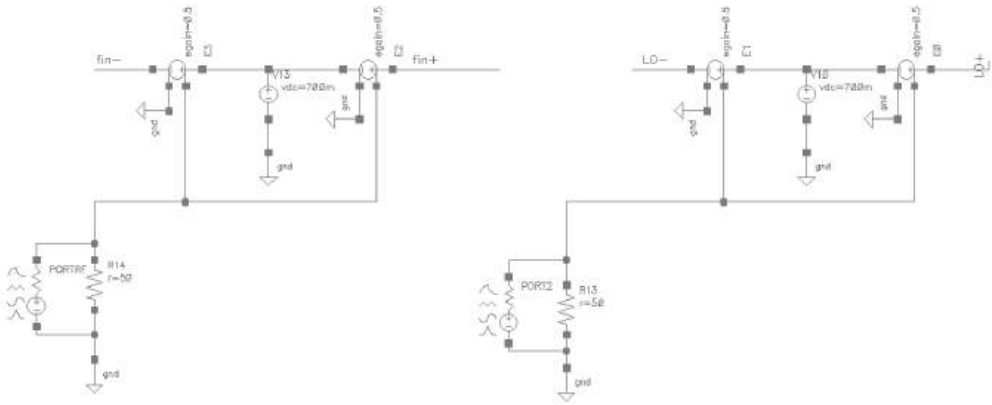


Figure 4.1.2 - RF and LO ports setup

4.1.4 Simulations

DC simulation.

After a small optimization, we can see that the switching works well:

- Currents of the ON pair are 800uA, so half of the tail current
- OFF pair conducts almost zero current
- RF transistors' gm value as expected

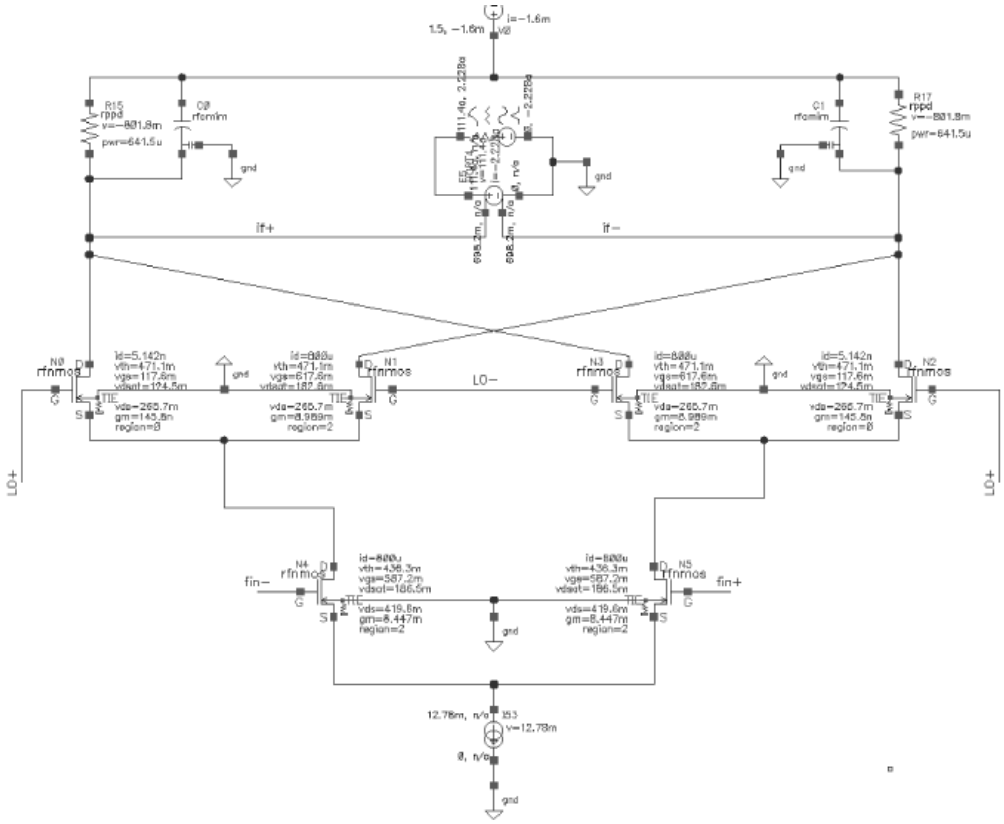


Figure 4.1.3 - DC operating points

Tran Analysis

RF = 3.1 GHz, LO = 3 GHz, IF = 100 MHz

Rise time is about 1.5ps. So we can say that switching front is fast. Switching is working as expected. It was optimized from the previous simulation of 3ps.

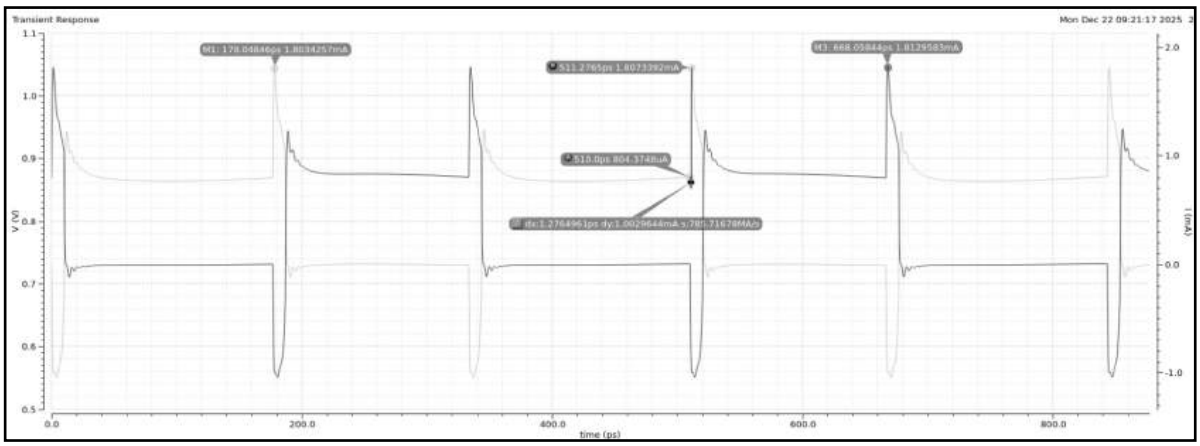


Figure 4.1.5 - LO, RF and Current steering.

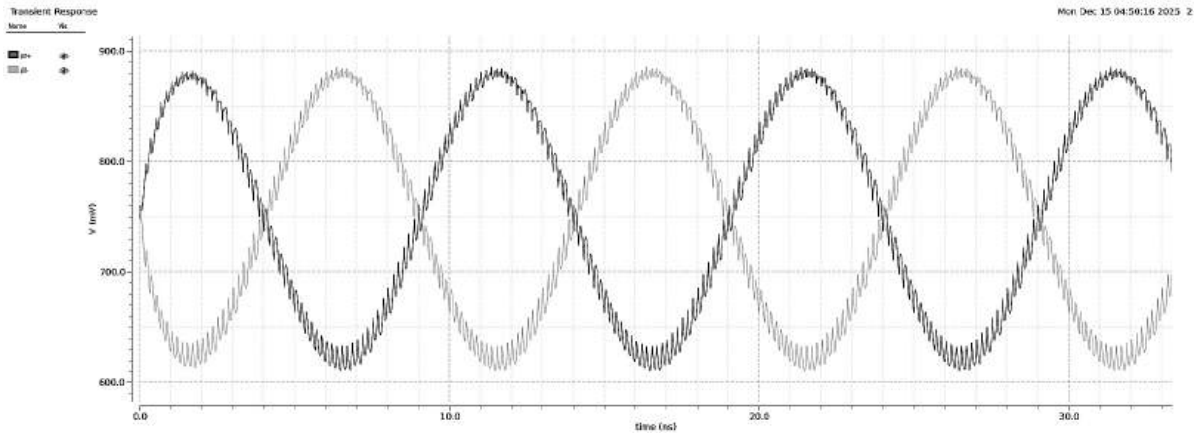


Figure 4.1.4 - IF Signal SSB

We can see exactly DC point at = 750mV. RF differential pair transistors are operating in saturation and strong inversion. LO transistors working as switches. Vov is very low is 15mV. Current steering is perfect Id/2. Not working pair of transistors is off.

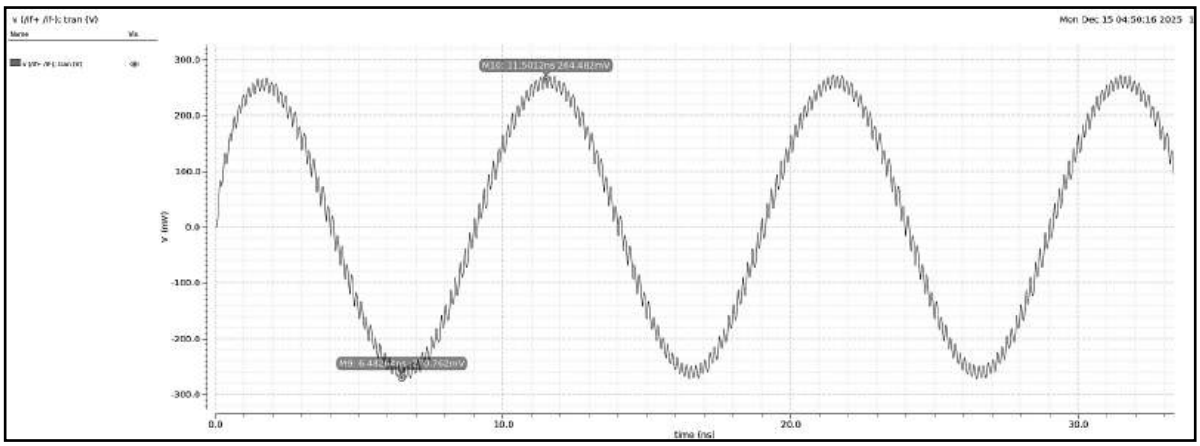


Figure 4.1.7 IF Differential output

We can see the pros of working with differential signals:

- no DC offset
- Doubled voltage swing
- Cleaner sinusoid

LO Power vs Conversion Gain (PSS+PAC)

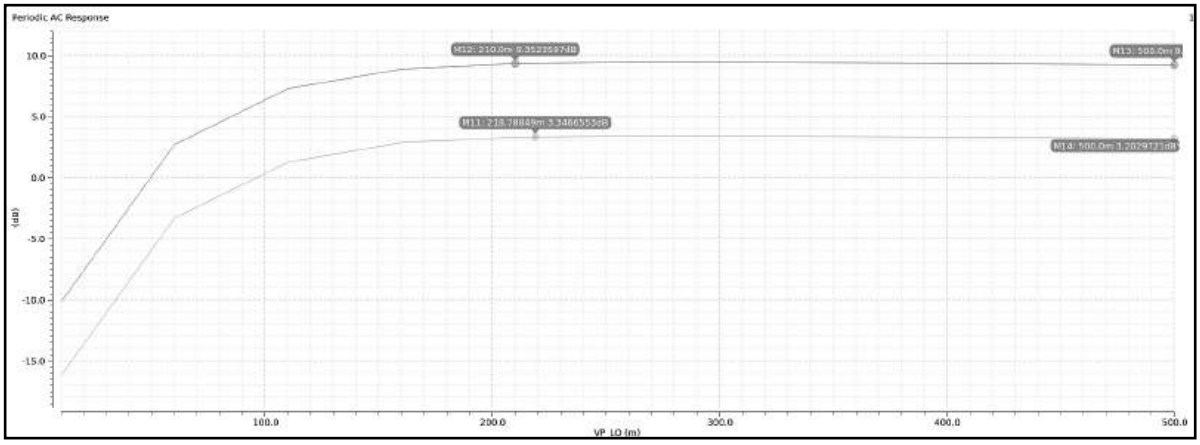


Figure 4.1.8 - LO power sweep SSB and DSB

Measuring mixer LO leakage and RF to IF isolation

We can measure the conversion gain using hb (Harmonic Balance) by applying the signal that causes the frequency conversion (the LO) in a hb analysis and follow this with HBAC (Harmonic Balance AC) to measure the small-signal conversion gain. This will also be used to measure RF to IF isolation. Because HBAC is based

on the hb result with all the harmonics that hb solved for, the mixing products produced by mixing the input frequency with any or all of those harmonics can be calculated with HBAC.

According to Cadence, HB solves for the steady-state solution produced by the LO and captures the nonlinearity of the mixer. Hb calculates the nonlinearity in the frequency domain as a series of harmonics.

The HBAC analysis calculates the conversion gain based on the nonlinearity created by the LO. HBAC is also used to calculate the RF to IF isolation. This measurement is not a simple AC frequency response. It is the frequency response from RF to IF with the LO applied to the mixer.

HBAC is a small-signal analysis. It is nonlinear in the sense of being able to take into account the frequency conversions created by the LO. According to Cadence - in practice, HBAC calculates the correct conversion gain for the cases where the RF input causes little compression (that is, the input is 10dB or more below the 1dB compression point)

RF signal is 0 GHz here, and LO Signal is 3GHz. The beat frequency signal is 3GHz. IF leakage is measured according to beat frequency.

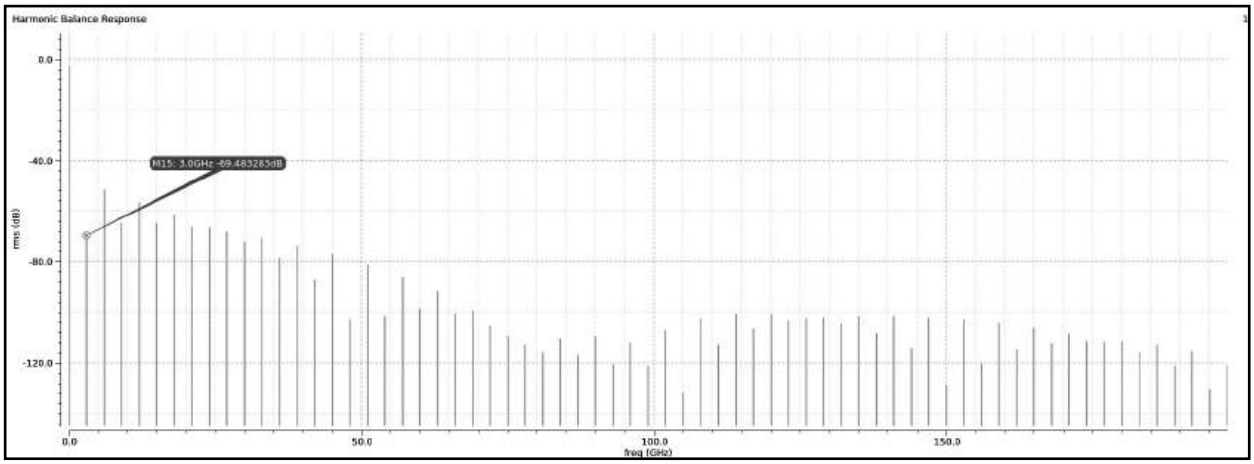


Figure 4.1.9 - LO to IF leakage

RF to IF isolation is measured with HBAC analysis. and measures the gain from input to output with no frequency conversion. This is due to RF to IF leakage.

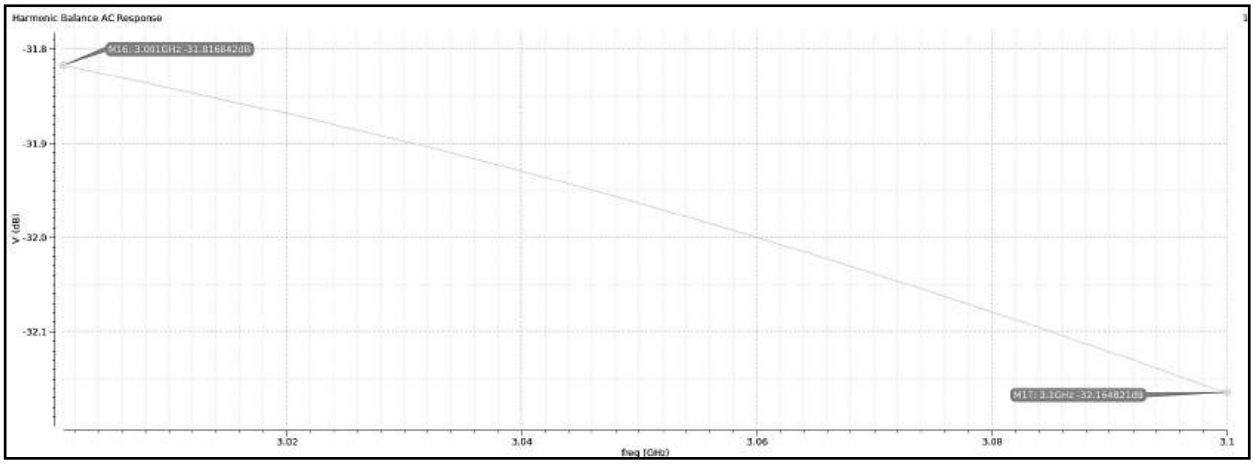


Figure 4.1.10 - RF to IF isolation

Conversion Gain - HB Analysis.

Harmonic balance and HBAC analysis performed to simulate conversion gain, Voltage Conversion Gain versus the Output frequency. When the IF is 1-100MHz. It rolls off at higher frequencies due to the degraded input match as the input moves above 3.001GHz.

We can see how the conversion gain degrades at a higher RF and LO frequencies. So we can see that Gilbert Cell probably is not the best choice for wideband mixing. We can see it when perform tran simulation at this frequency.

The conversion gain has been measured as to a SSB. DSB gain will be twice higher approx.

Top left: LO to IF leakage. Bottom-left: RF to IF isolation. Top-right: Conversion gain. We see that the conversion gain degrades at higher frequencies.

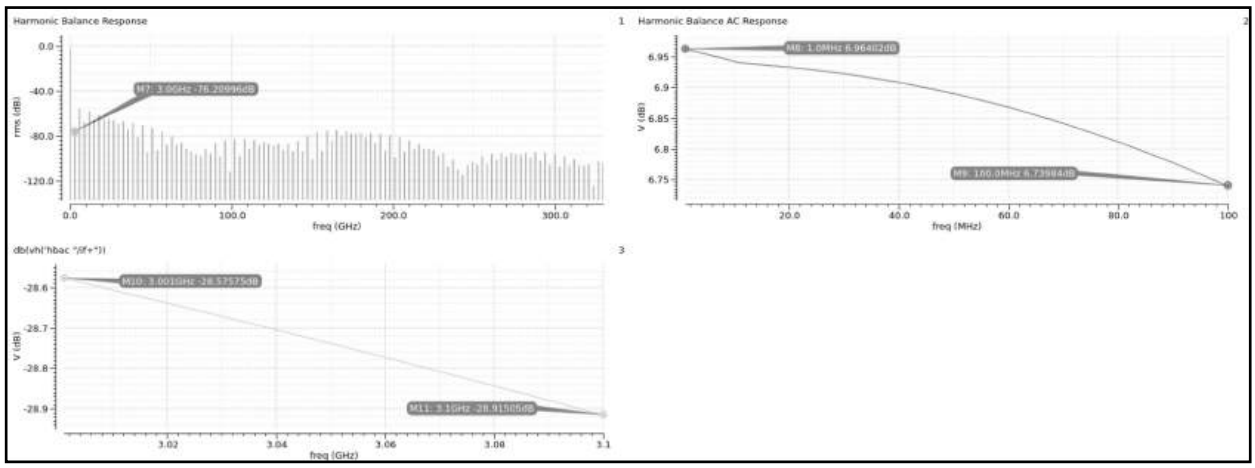


Figure 4.1.11 -
Conversion Gain at 3 GHz to IF 1-100MHz. LO to IF leakage. RF to IF isolation

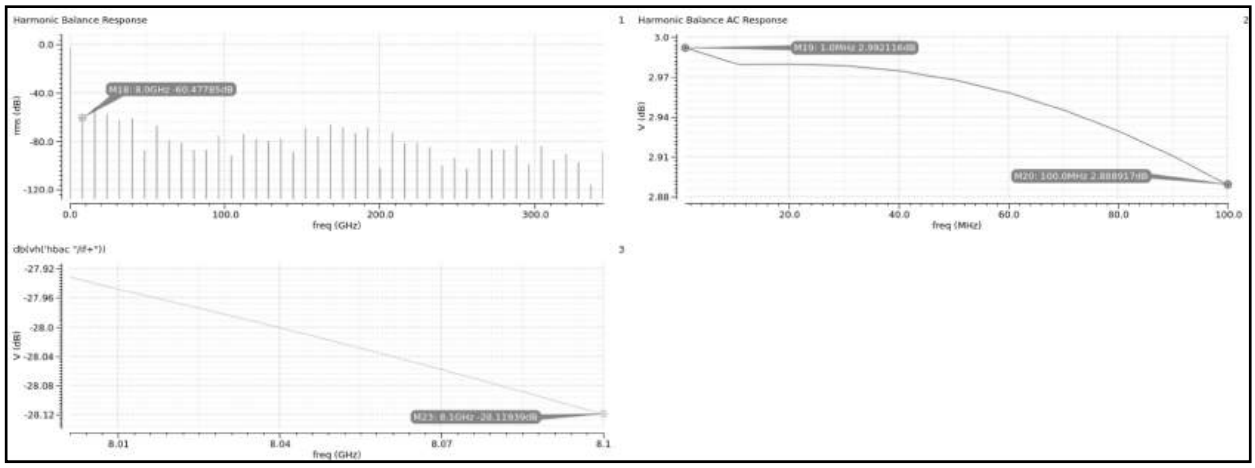


Figure 4.1.12 -
Conversion Gain at 8 GHz to IF 1-100MHz. LO to IF leakage. RF to IF isolation

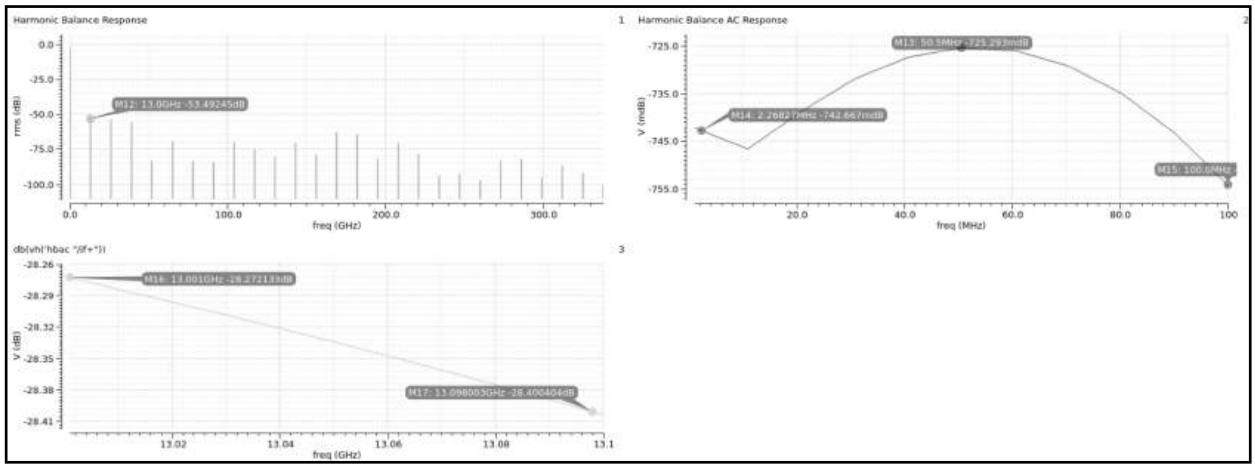


Figure 4.1.13 -
Conversion Gain at 13 GHz to IF 1-100MHz. LO to IF leakage. RF to IF isolation

Noise Figure PAC + PNOISE analysis

The noise performance of a mixer is measured by the degradation of the signal-to-noise power ratio (SNR) after mixing. The input SNR is measured at the RF frequency, while the output SNR is calculated at the IF frequency. Mixing translates down both signal and noise at both the desired channel and its image channel. In the cases where the image frequency does not contain a useful signal, the noise power is doubled after mixing, while the signal power remains constant (both referred to the input). Therefore, even a noiseless mixer has 3 dB NF. Direct conversion mixer, where IF is zero, is an exception because the image of the desired signal is itself. Therefore, in this special case, the signal power and the noise power go through the same process, and SNR remains unchanged, i.e., NF=0. In practice, transistors and resistors of the mixer add noise and increase NF, however we can still say that double sideband NF (NFDSB) is 3 dB lower than single sideband NF (NFSSB).

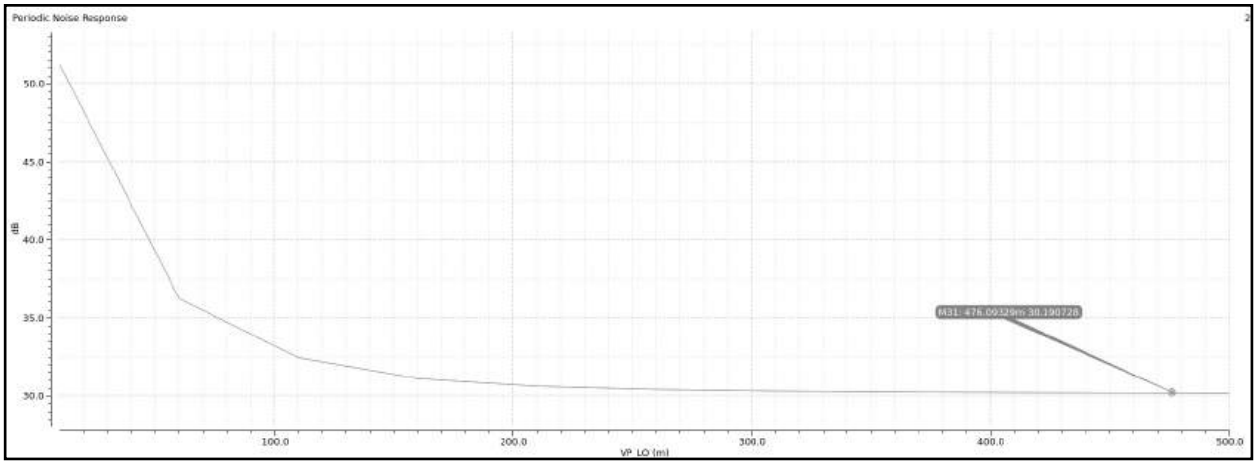


Figure 4.1.14 - 3GHz beat frequency - NF = 30dB

Device	Param	Noise Contribution	% Of Total
/N3	Rjunsnoise	1.45627e-05	9.54
/N2	Rjundnoise	1.45627e-05	9.54
/N2	Rjunsnoise	1.45627e-05	9.54
/N1	Rjundnoise	1.45627e-05	9.54
/N1	Rjunsnoise	1.45627e-05	9.54
/N0	Rjundnoise	1.45627e-05	9.54
/N0	Rjunsnoise	1.45627e-05	9.54
/N3	Rjundnoise	1.45627e-05	9.54
/C1/rskin	rn	1.16602e-05	6.12
/C0/rskin	rn	1.16602e-05	6.12
/C1/rmim	rn	9.10809e-06	3.73
/C0/rmim	rn	9.10809e-06	3.73
/N3	Rwellnoise	2.62533e-06	0.31
/N3	Rbulknoise	2.62533e-06	0.31
/N2	Rwellnoise	2.62533e-06	0.31
/N2	Rbulknoise	2.62533e-06	0.31
/N1	Rwellnoise	2.62533e-06	0.31
/N1	Rbulknoise	2.62533e-06	0.31
/N0	Rwellnoise	2.62533e-06	0.31
/N0	Rbulknoise	2.62533e-06	0.31

Integrated Noise Summary (in A) Sorted By Noise Contributors
Total Summarized Noise = 4.71394e-05
No input referred noise available
The above noise summary info is for pnoise_src data with VP_LO = 0.5

Figure 4.1.15 - Top 20 noise sources summary

We can see a significant Noise figure. Let's do a noise summary report In the noise summary report, we can see that the main noise contributors are our switching quad transistors.

We can assume that, due to their channel width of 400 µm the parasitic capacitors are very big. Let's try to make them smaller to 50 µm and 8 fingers and simulate again.

4.2 Noise and LO switching opmization.

We can see an improved noise figure by making the transistors less in with. But it is still too high and not what we expected.

We also have an improved conversion gain because our switch quad transistors are now operating in the saturation region. With 146mV overdrive instead of 20mv. The width has been modified from 400µm to 50µm to achieve this result. The simulation results can be justified from these plots.

Let's perform Tran analysis so we can see how the current steering changed. We can see it is 1.5ps now, so 10x times faster.

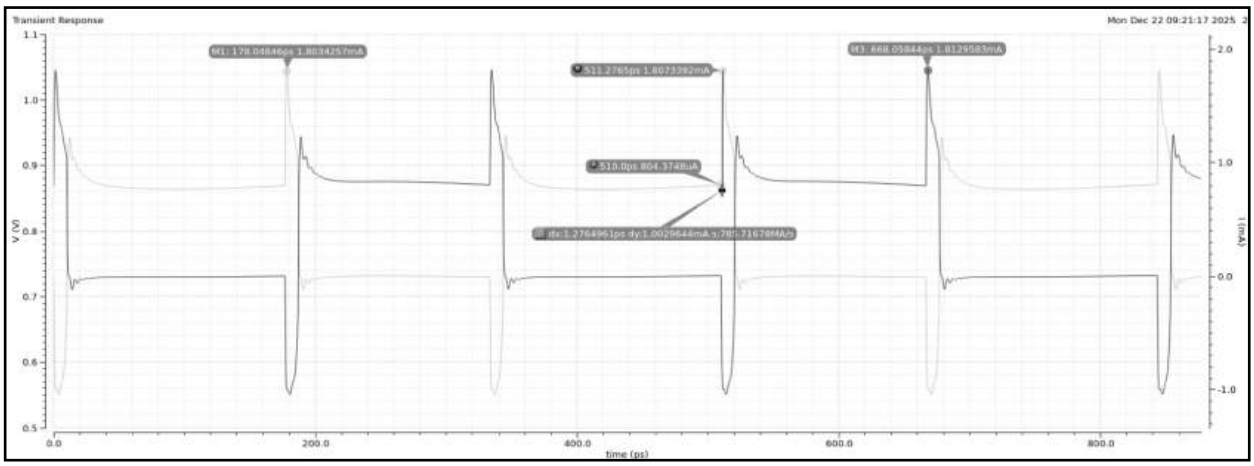


Figure 4.2.2 - Improved Current steering

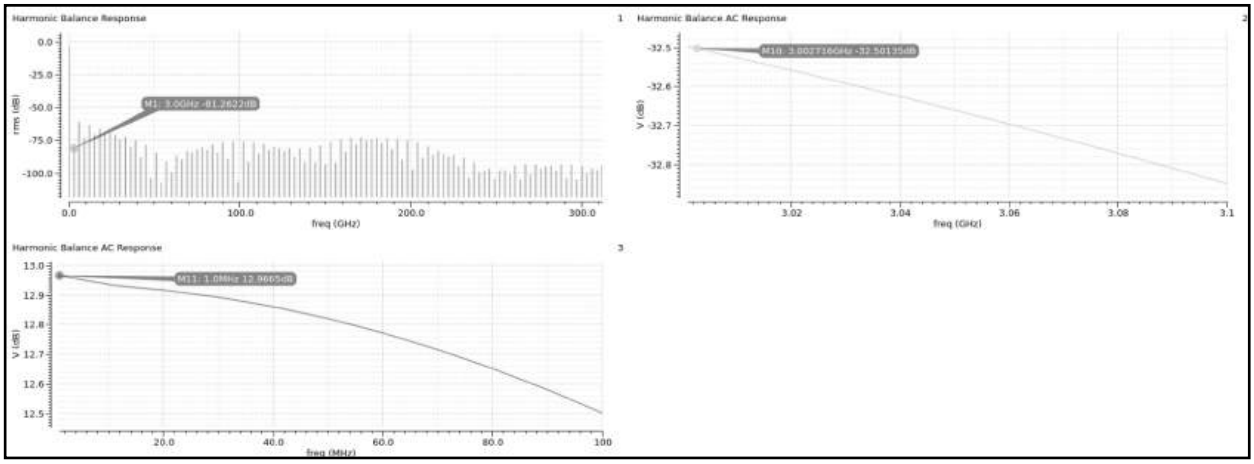


Figure 4.2.1 - IF frequency Improved conversion gain with LO 3 GHz

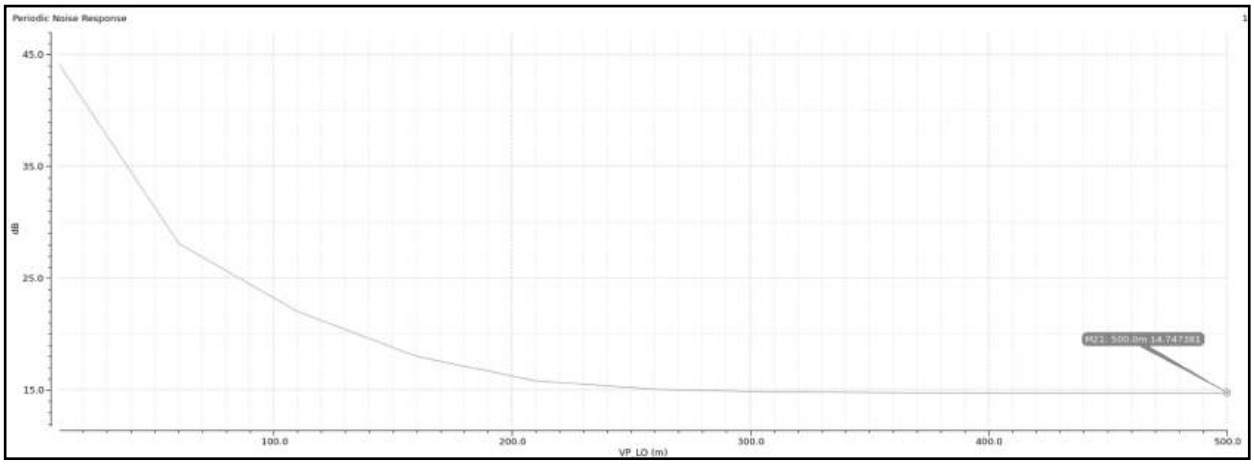


Figure 4.2.3 - Improved DSB Noise figure versus LO power at 3 GHz

From the above plots, we can see improved LO to IF isolation, 10x faster LO rise time, 2x better NF - now it is 14.7dB. Conversion gain is nearly the same at this frequency, but increased at higher Frequencies.

Based on the above, we can conclude:

The quality of switching in a mixer is determined by the duration for which the LO switching devices operate near the threshold voltage during commutation. During this interval, the devices temporarily enter saturation, exhibit high transconductance (leading to increased channel noise), and efficiently couple device noise to the output, while only partially steering the signal current. This noise coupling includes both thermal and flicker noise components.

Both the LO rise/fall time and the LO voltage swing influence this behavior. The LO rise and fall times determine how quickly the gate–source voltage traverses the threshold region, thereby setting the duration of the saturation interval. In addition, the LO voltage swing affects the effective transition speed at the switching devices, since larger overdrive enables stronger charging and discharging of the device parasitic capacitances and reduces the time spent near threshold.

The LO voltage swing also determines how deeply the LO switching devices enter the triode region after commutation. If the LO swing is insufficient and only marginally exceeds the threshold voltage, the devices exhibit high and nonlinear on-resistance and incomplete current steering throughout the LO half-cycle.

In addition to noise, non-ideal LO switching directly impacts mixer linearity. When the LO switching devices operate near threshold or fail to enter deep triode operation, their finite and nonlinear conduction causes the current steering process to become dependent on the RF signal amplitude. In this regime, voltage drops across the switching devices and variations of the switch tail node voltage follow the instantaneous RF current, thereby modulating both the effective conduction of the switches and the drain–source voltage of the RF transconductance devices. As a result, the differential output voltage is no longer a linear function of the RF input amplitude, leading to gain compression and the generation of intermodulation products.

Non-ideal switching also degrades conversion gain, but through a distinct mechanism. With finite switch impedance and incomplete commutation, the RF transconductance current is not fully converted into a differential output component. During overlap conduction and throughout the LO half-cycle, a portion of the RF current appears as common-mode and therefore does not contribute to the differential IF output. Consequently, the amplitude of the effective fundamental mixing component is reduced, resulting in a measurable degradation of conversion gain.

Linearity

1dB Compression Point, Desensitization, and Blocking of the receiver.

1dB Compression Point

All circuits reach a compression point. The large signal effects at this point cause the gain to stop increasing linearly. Since this is a large-signal effect, a large-signal analysis is required. When measuring the 1dB Gain compression point, the idea is to sweep the input power over a range of power levels and then plot the output power versus the input power. From the plot, the 1dB compression point can be determined (the 1dB compression point is the input signal level at which the receiver gain drops 1dB when compared to the ideal linear gain).

Desensitization and Blocking of the receiver

Receiver desensitization interference occurs when a strong out-of-channel signal overloads a receiver front end and thereby reducing the effective sensitivity to weaker in-channel signals. For desensitization measurement, the frequency component set in the RF input port is considered the RF blocker frequency. In our case, it is 3.004GHz. And we are measuring the conversion gain from 3.0002GHz to 200KHz IF. LO frequency is set to 3 GHz.

We will also perform an HB noise simulation versus RF power. Because pRF is being swept in HB, the noise figure can be measured as a function of input power (pRF).

Here we can see that our 1dB compression point is -8.5dB at IF 4 MHz.

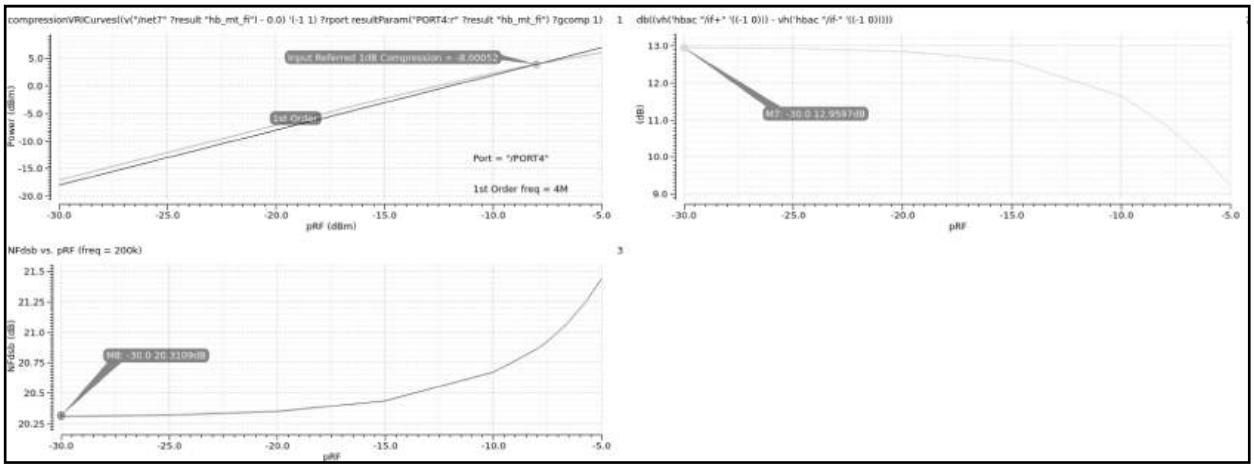


Figure 4.2.4 -
1dB compression point. Noise and conversion gain vs RF power blocker.

Note the trend in conversion gain and noise figure. As expected, the noise figure goes up, and the conversion gain goes down with increasing RF blocker power (pRF).

The second graph is the conversion gain to IF 200KHz when the RF signal is at 3.0002GHz, and another signal is at 3.004GHz. The power of this signal we are sweeping and looking at how the conversion gain to IF 200KHz goes down, while the signal 2 power goes up.

3rd graph noise figure represents the same. And we can see how NF degrades, while the blocking power Frequency goes up.

3rd order Intercept Point (IP3) and 2nd order intercept point

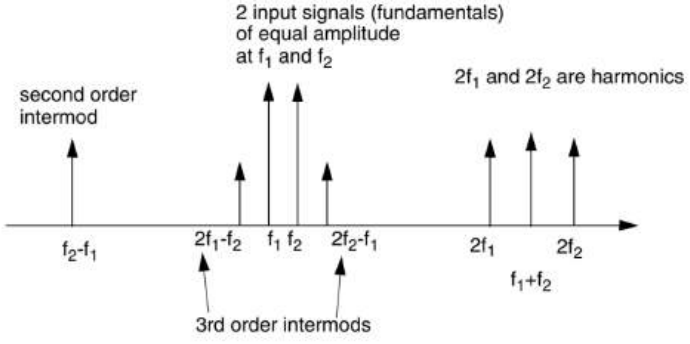


Figure 4.2.5 - Intermodulation Distortion Products

In the frequency domain, third-order products are the intermodulation distortion products between one of the fundamental signals and the second harmonic of the other signal[15].

The presence of two or more tones in a nonlinear circuit generates intermodulation products. Many of the spurious tones are out-of-band and cause no problems. However, the third-order tones are nearest to the fundamental and are likely to fall in-band. They add distortion to the output signal. IP3 is a metric or figure of merit for linearity that is used to describe the intermodulation performance of a mixer.

We measure this 2 fundamental tones at 3.004 and 3.005 GHz with the same amplitude and sweep second tone power.

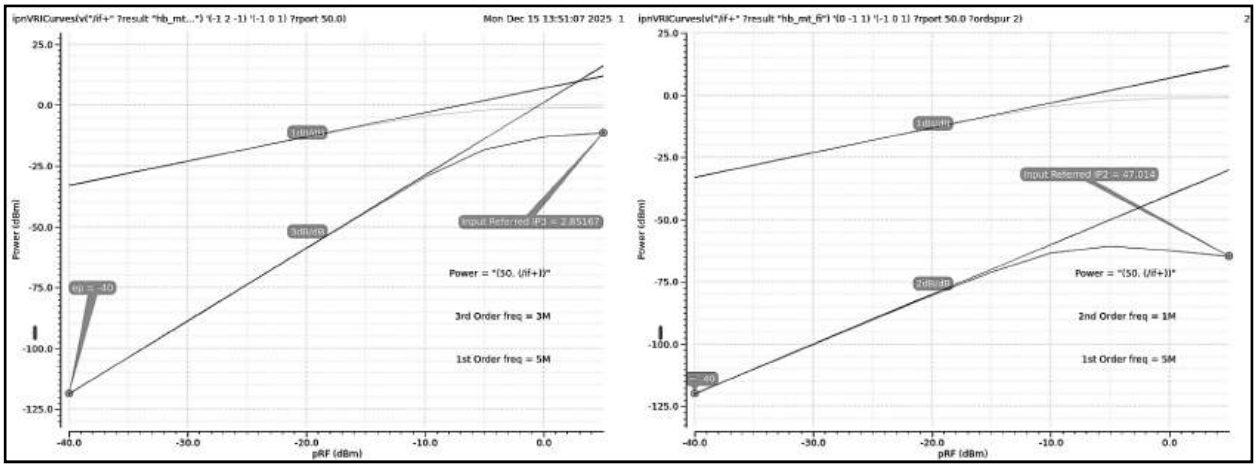


Figure 4.2.5 - on the right - IP3. On the left - IP2

Our 1st order harmonic = IF signal = 5 MHz

Two things we can justify here:

- IP2 - 1 MHz double balanced topology works, and we can see IP2 far away (right graph) 47dBm.
- IP3 - 3 MHz is relatively good as it distorts only with the signal power of 2.8dBm.

[15] Figure 4.2.5 is taken from (6)

5. Results Overview.

Here, the improved results will be presented, with noise optimization and improved conversion gain.

IF Frequency is always used 100MHz for these simulations

Frequency (Hz) LO	Conversion Gain DSB (dB)	Noise Figure DSB (dB)	LO-IF leakage (dB)	RF-IF isolation (dB)
3GHz	12.9	14.7	-81	-32
8GHz	10.6	19	-65	-31.8
13Ghz	8.5	22	-58	-31

Table 5.1 - Conversion gain and Isolation. IF Frequency 100MHz

Frequency (Hz) LO	1dB Compression point	Conversion gain vs Blocking Frequency power	Noise figure (DSB) vs Blocking Frequency
3GHz	-8.5 dBm	12 dB to 9 dB	20 - 21 dB
8GHz	-8.1 dBm	10 dB to 8.7 dB	23.8 - 25 dB
13Ghz	-7.3 dBm	8.8 dB to 5.2 dB	27.4 - 28.6 dB

Table 5.2 - 1dB Compression point vs RF power from -40 to-5dBm.
Blocking frequency 200 KHz.
IF Frequency 4MHz.

Frequency (Hz) LO	IP3 (dBm)	IP2 (dBm)
3GHz	2.8 dBm	47 dBm
6GHz	4.68 dBm	51 dBm
13Ghz	6.7 dBm	54 dBm

IP3 and IP2. 1st order frequency 3 MHz, 2nd order = 1 MHz. 3rd order = 5MHz

6. Takes

As a results of this work we can see the following:

1. Conversion gain, Noise degrades at a higher frequencies.
2. The quality of switching in a mixer is determined by the duration for which the LO switching devices operate near the threshold voltage during commutation.
3. Linearity in a opposite side improving when the frequency goes higher.
4. Noise figure improves, while we increase over voltage of both, switching quad and RF diff pair and decrease channel width.
5. Bigger channel width leads to higher gm and higher gain, but result is the degradation of NF.
6. In Gilbert Cell mixer conversion gain depends of the gm of the RF transistors and RD (load resistor)
7. Top noise contributors are switching quad transistors.
8. The most critical takes are for the LO switching transistors is that:
   - Higher over voltage - lower gm/Id - lower noise - lower gain
   - Lower over voltage - higher gm/Id - higher noise - higher gain

So as a general conclusion we can say reducing W/L at constant current increases overdrive voltage but reduces transconductance, so reduce conversion gain; noise figure improves only if the increase in overdrive is accompanied by an increase in transconductance, usually through higher bias current. Based on the above we can conclude that the main tradeoff in this topology is conversion gain vs noise figure. The next steps of the optimization can be:

1. To plot NF vs gm/Id.
2. Optimize W/L ratio
3. Optimize biasing current

Sources

(1) Behzad Razavi *"RF Microelectronics Second Edition"*, 2012. Chapter 6 - Mixers. Pages 337-408

(2) G. Tasselli, F. Alimenti, A. Fonte, D. Zito, L. Roselli, D. De Rossi, A. Lanatà, B. Neri, A. Tognetti *"Wearable Microwave Radiometers for Remote Fire Detection: System-on-Chip (SoC) Design and Proof of the Concept"* in IEEE // https://www.researchgate.net/publication/23931990_Wearable_Microwave_Radiometers_for_Remote_Fire_Detection_System-on-Chip_SoC_Design_and_Proof_of_the_Concept

(3) Rahul Sharma, Abhay Chaturvedi, and Manish Kumar *"A Comparative Study Of Different Types Of Mixer Topologies",* Department of Electronics and Communication Engineering, Institute of Engineering and Technology, GLA University. India. Semanticscholar https://pdfs.semanticscholar.org/a67d/f3b21a461f712145bb40a6e35c4b36b65263.pdf

(4) Chun-Lin Kuo; Bo-Jr Huang; Che-Chung Kuo; Kun-You Lin; Huei Wang *"A 10–35 GHz Low Power Bulk-DrivenMixer Using 0.13 μm CMOS Process",* in IEEE https://ieeexplore.ieee.org/document/4538239

(5) C.-S. Lin; P.-S. Wu; H.-Y. Chang; H. Wang "A 9-50-GHz Gilbert-cell down-conversion mixer in 0.13-μm CMOS technology." in IEEE https://ieeexplore.ieee.org/document/1626265

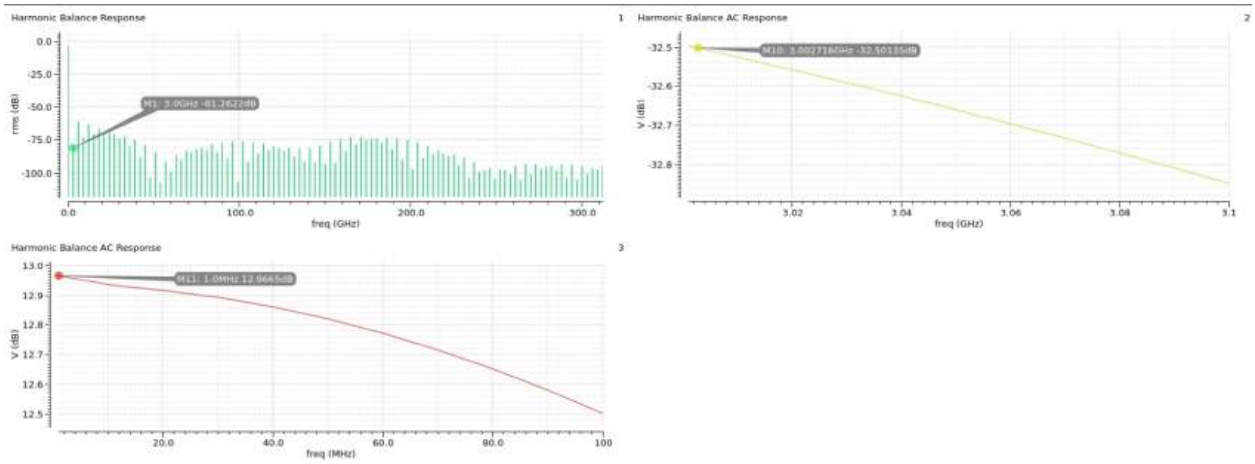
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(7) CadenceWorkshops. "*Spectre Circuit Simulator and Accelerated Parallel Simulator RF Analysis in ADE Explorer Workshop"*, Product Version 25.1, July 2025. Page 331. KSE Engineering school access.

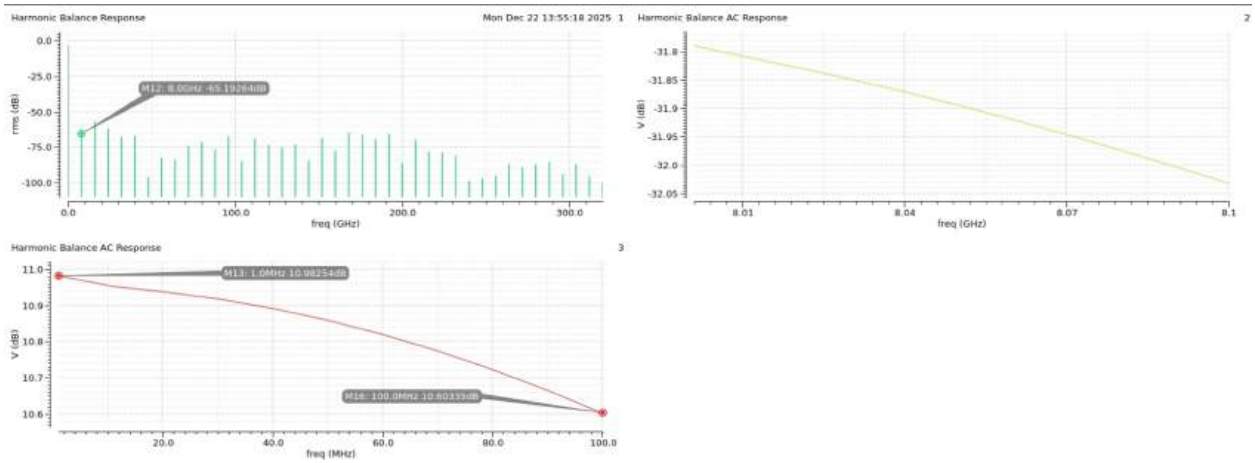
Appendix A

A. DSB Conversion gain to IF 1-100 MHz, LO-to-IF leakage, and RF-to-IF feedthrough at IF 1-100MHz. HB and HBAC simulations.

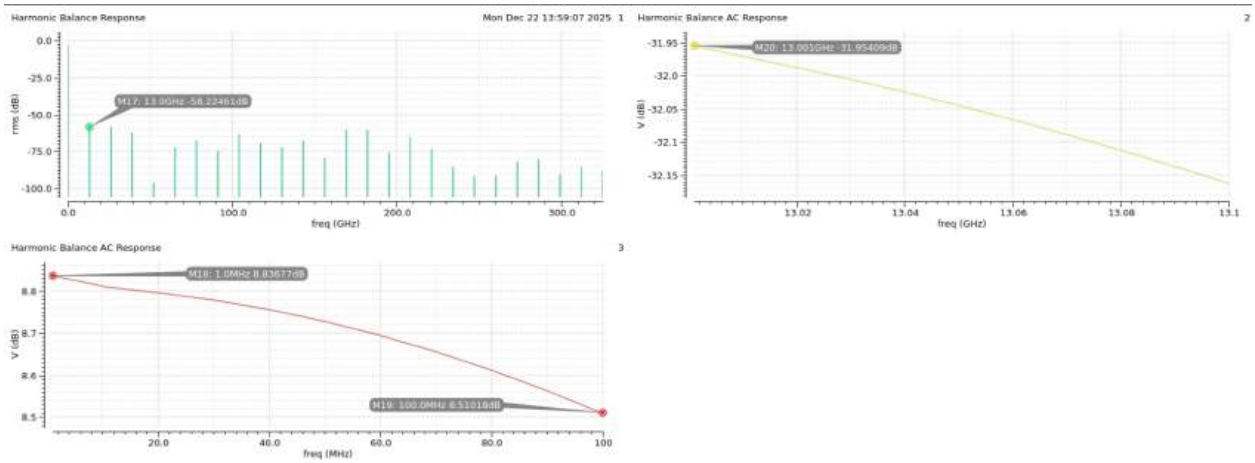
3 GHz



8 GHz

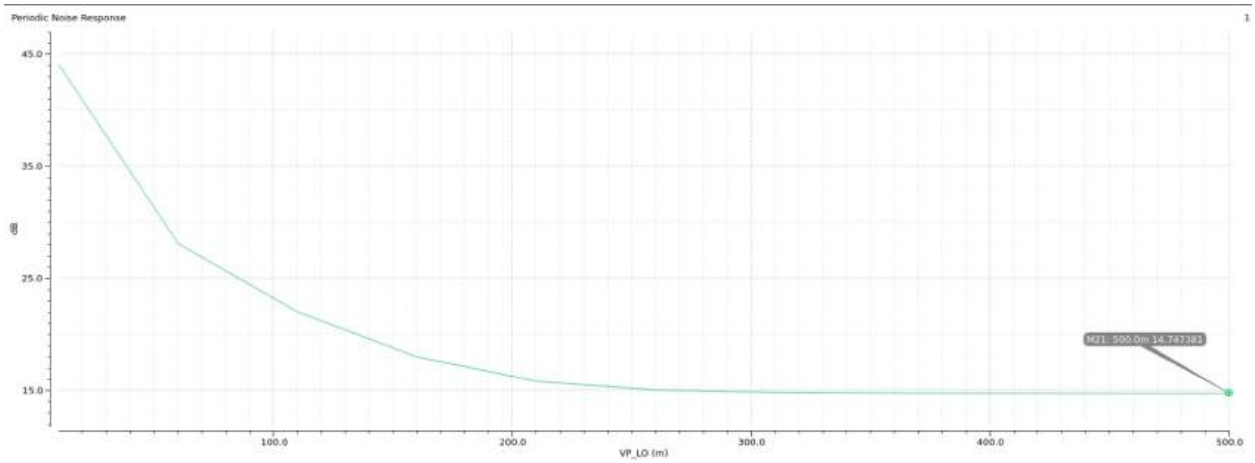


13 GHz

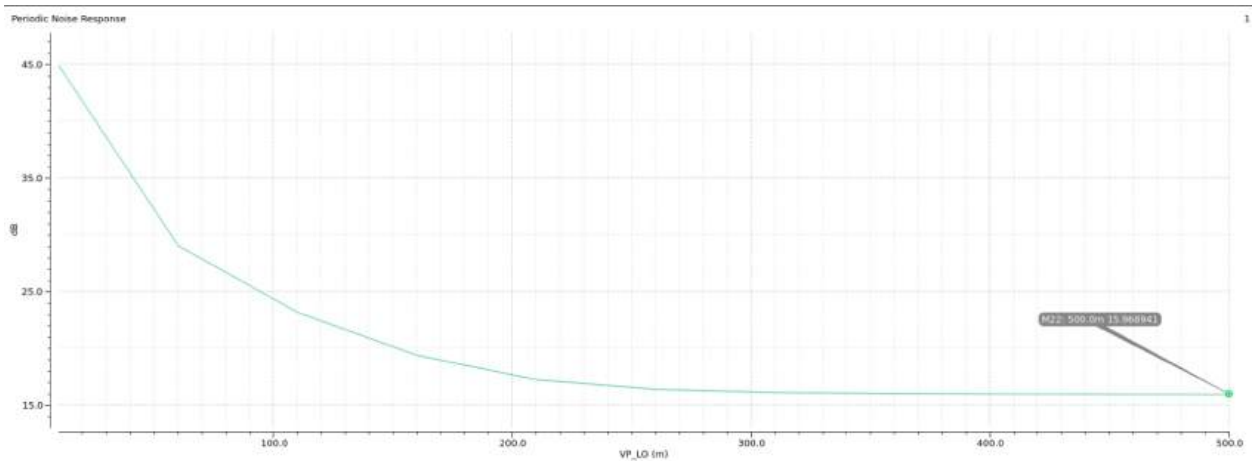


B. Noise Figure (DSB) vs LO power. PAC+Pnoise simulations

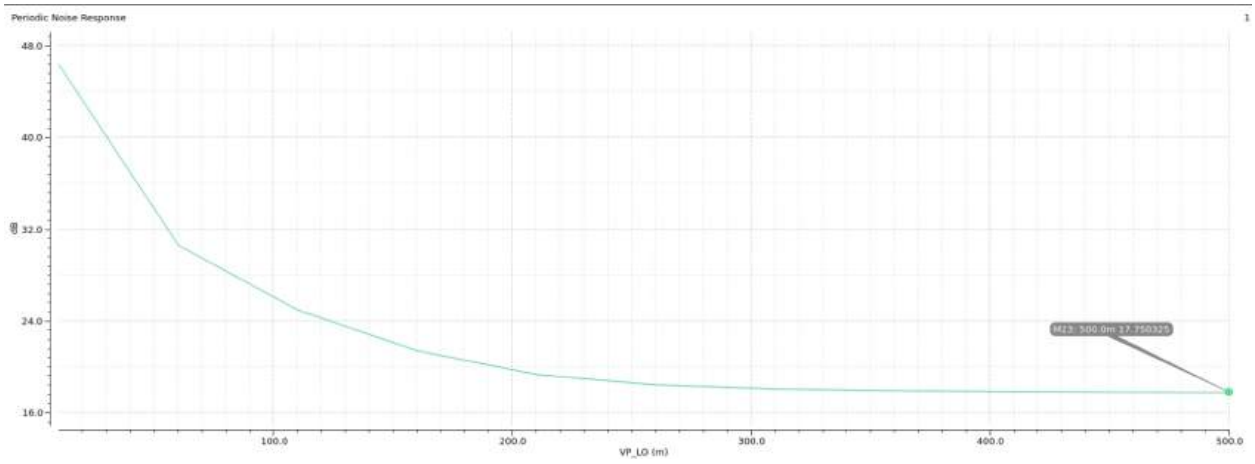
3 GHz



8 GHz

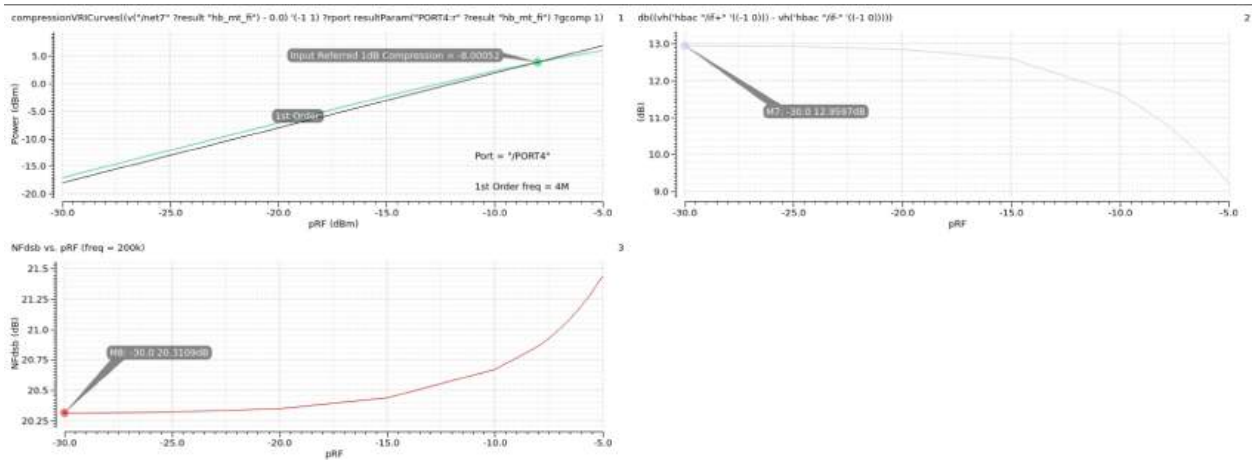


13 GHz

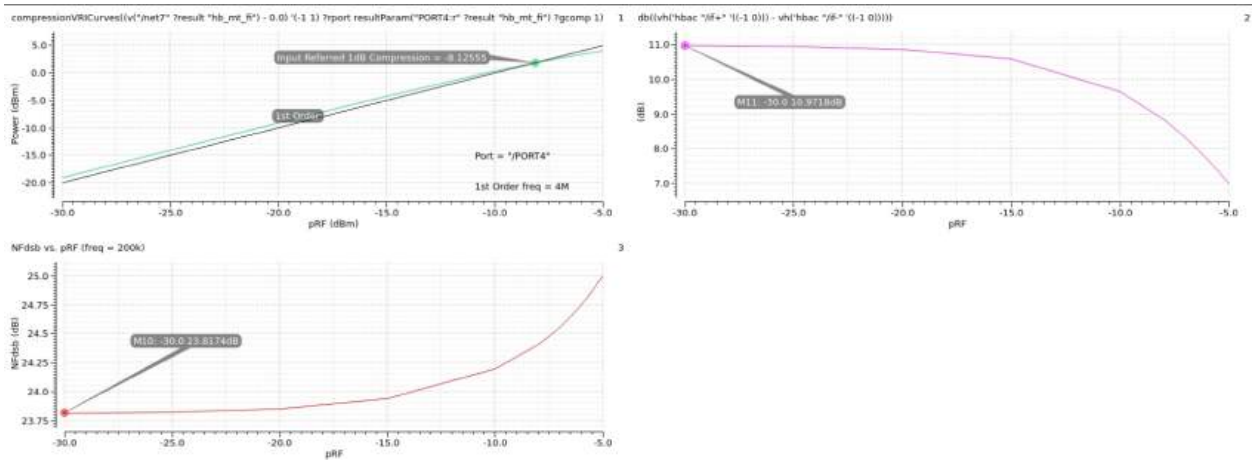


C. 1dB compression point vs RF power. DSB Noise and Conversion gain vs RF power blocker.

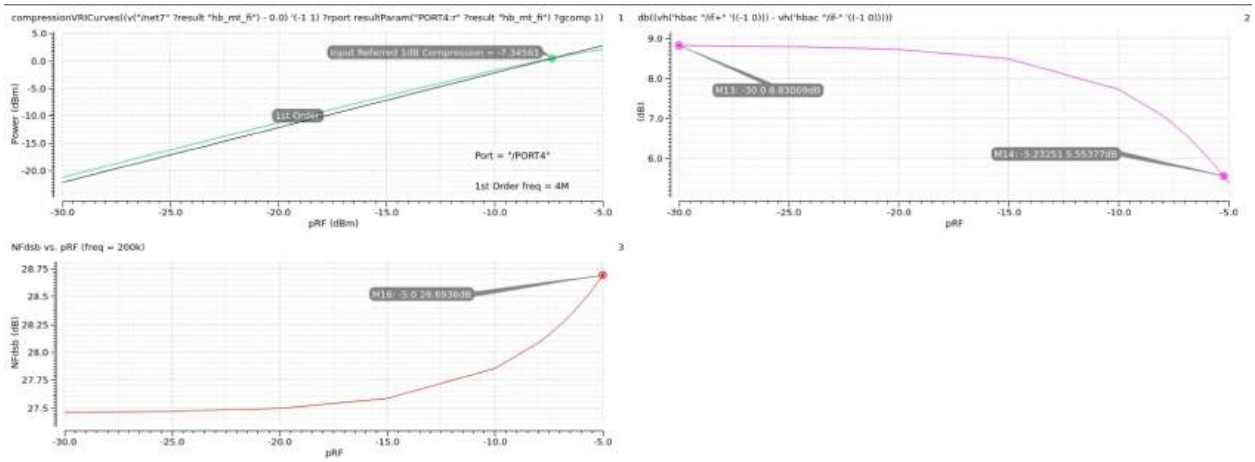
3 GHz, Blocking frequency is at 3.0002 GHz.



8 GHz, Blocking frequency is at 8.0002 GHz.

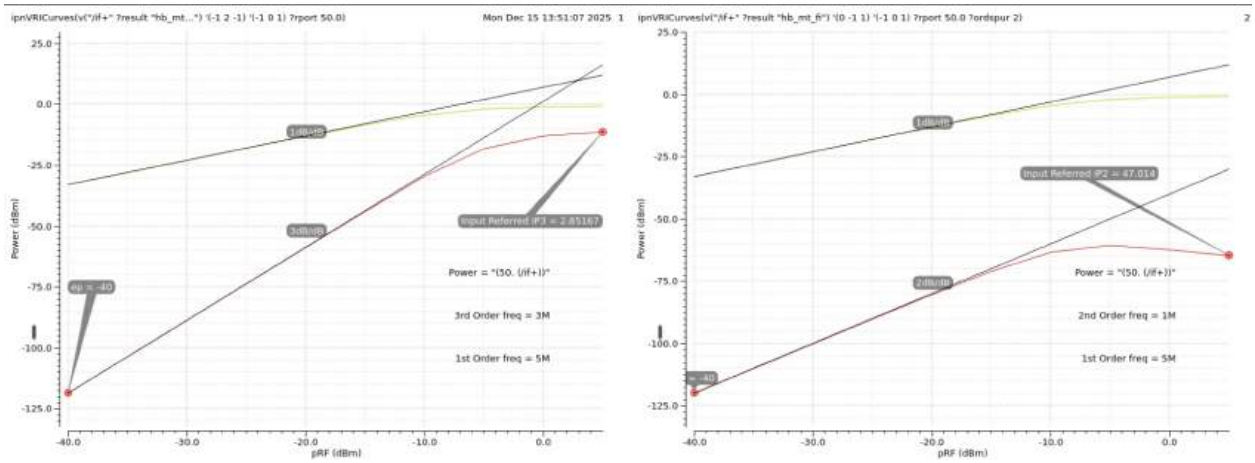


13 GHz, Blocking frequency is at 13.0002 GHz.

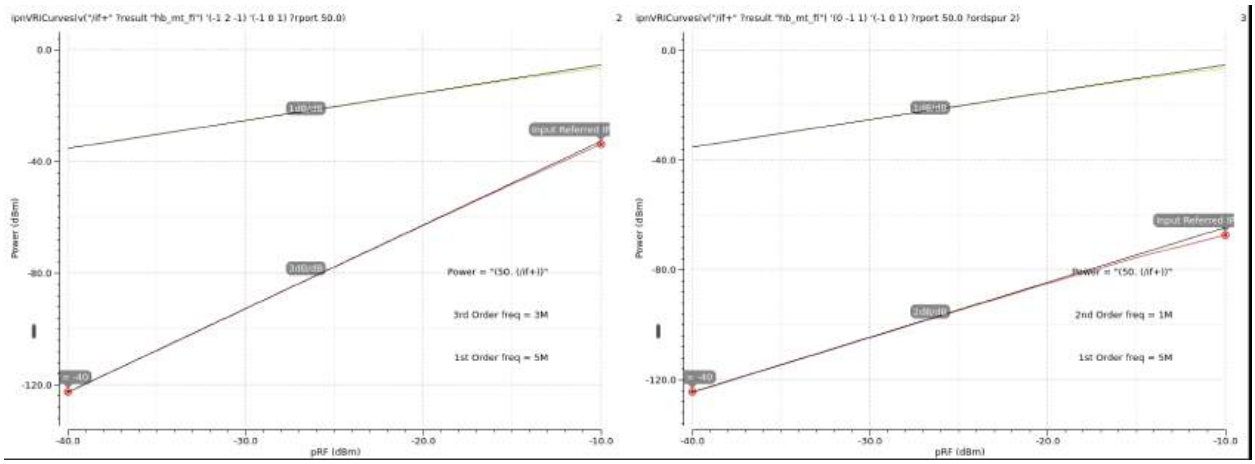


D. IP3 and IP2 intermodulation points.

3 GHz



8 GHz



13 GHz

