School of Engineering

Micro- and Nanoelectronics Programme

Master's Thesis

Feasibility of opamp-based gate driver with EMI optimization

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ABSTRACT

As power converters migrate toward higher switching frequencies to improve power density, the rapid voltage and current transitions (dV/dt and di/dt) inherent to hard-switching topologies have become a dominant source of electromagnetic interference (EMI). This thesis investigates the effectiveness of active gate-driver topologies in improving these emissions at the source, specifically by shaping the gate-source voltage (Vgs) shape of the power MOSFET.

Three distinct driver architectures are designed and analyzed in a 0.13 um CMOS technology: a baseline conventional push-pull driver, a digitally controlled segmented driver, and a novel closed-loop operational transconductance amplifier (OTA) based driver.

Keywords: Gate Driver, Electromagnetic Interference (EMI), Active Gate Shaping, OTA, Segmented Driver, Slew Rate Control, Power Electronics.

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CHAPTER 1 INTRODUCTION

1.1 Motivation

The 21st century can be defined by the rapid growth of the sphere of technology, the expansion of electric vehicles' market, growth of renewable energy infrastructure, and AI taking over all spheres of lives. AI relies on huge datacenters, some of which will soon require their own nuclear power plant to operate. [1] As of 2025, 9 of 10 world's most expensive companies are related to technologies [2]. The fundamental part of their operation and growth relies on development of power management solutions, especially, switching power conversion circuits whose job is to convert energy from one way to another. Power MOSFET is the key element of power conversion. It can be simply described as a high speed switch. Ideally, the MOSFET would show instant switching and no power dissipation. The pursuit of making the switching more efficient has inevitably led to the increase of switching speed, however, it cannot be increased indefinitely. Driving a power MOSFET requires overcoming a fundamental problem of charging a capacitive load on the gate as fast as possible. To do this, a specialized circuit called a gate driver is utilized.

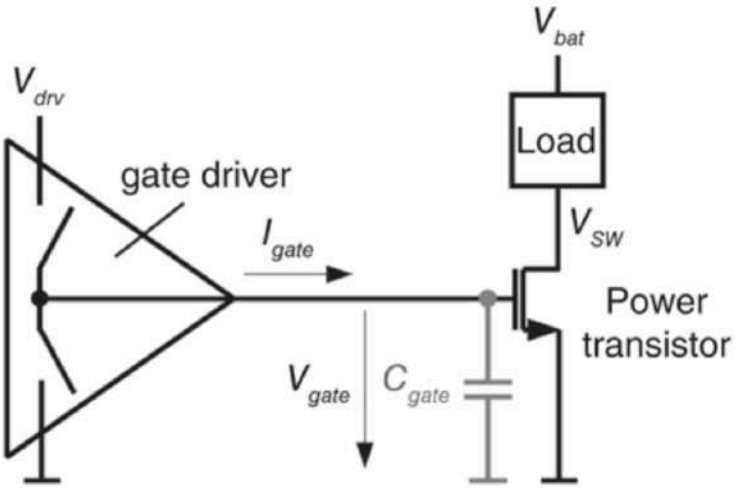


Figure 1.1 – A typical gate driver [3, p. 153]

Switching currents into inductive loads at high speed becomes a source of electromagnetic interference (next EMI) which limits the performance of nearby electronic equipment.

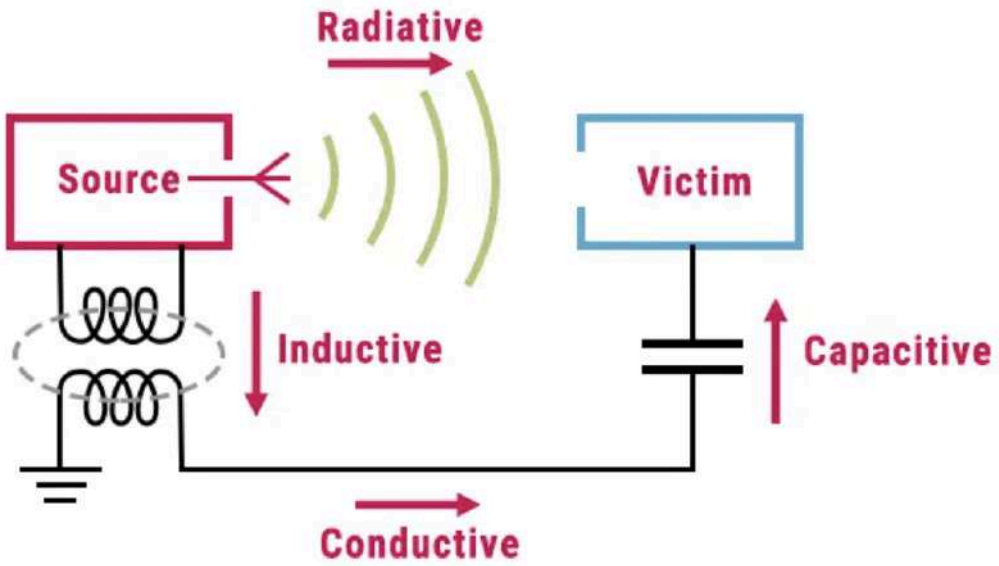


Figure 1.2 – Inductive, conductive, capacitive, and radiative EMI in a system [4].

This leads to the major trade-off of power electronics. A fast switching driver may be efficient but it presents noise that contradicts regulatory standards. A slow driver is inefficient, dissipates lots of energy which results in a need for thermal management, growth in size and cost. On one side there is efficient switching and on the other side is EMI compliance.

The problem is, a simple MOSFET switch is not enough for today's sophisticated needs. The so-called state-of-the-art gate drivers utilize clever techniques for controlling the switching speed, specifically shaping the gate voltage in a specific way to achieve trade-offs between power losses and acceptable level of EMI [23].

1.2 The Core Problem: trade-off between efficiency and EMI

Fast switching can be defined as minimizing the time MOSFET spends in the saturation region. The downside of such fast switching is that it radiates

electromagnetic noise as each fast edge acts like a broadcast antenna, producing harmonics (high frequency components). Slow switching, on the contrary, spends more time in the saturation region of the transistor which results in an increase of switching losses, general decrease in efficiency and increased heat waste. Slow switching, however, creates less high frequency harmonics and less EMI. It should be noted that EMI, though not being a significant topic in academic studies, is a very serious limiting factor that should be accounted for. The reasons for this include:

- **System-wide interference:** High frequency noise from a power converter can interfere with the microcontroller, sensitive analog sensors or communication lines. In large and complex systems like data centers or electronic vehicles this may lead to system-wide failure.
- **Regulatory compliance:** electronic components, especially in the automotive world where humans' safety is a priority, have to pass strict regulatory compliance like CISPR 25 or FCC. These regulations set the limit on allowable emission level and it is prohibited to legally sell the device without complying with them.
- **Size of solution:** Passive filters are a traditional way of fighting EMI. They are usually expensive, heavy and quite large so it sounds reasonable to find ways to design devices that do not require such filters.

These reasons bring to the conclusion that it is not a matter of fast or slow but rather smart switching which is called slew rate control. Suppressing high frequency harmonics is made possible by managing dV/dt and di/dt of the switching moment or simply shaping gate voltage. This allows to sacrifice the minimum amount of energy in switching losses while achieving EMI compliance. An ideal system with minimized EMI concentrates its energy only at fundamental switching frequency.

1.3 Thesis Objectives and Contribution

The primary aim of this thesis is to explore and compare two existing gate drivers: the conventional push-pull and state-of-the-art (next SOA) technique of gate pulse shaping and additionally propose a new operational transconductance amplifier-based topology (next OTA) which may result in improved EMI.

The specific contributions of this research are:

- Design and simulation of a classic tapered push-pull driver to have a baseline for comparison (Discrete Fourier transform analysis) with other topologies.
- State-of-the-art analysis: an attempt to implement a segmented driver with multistep digital control.
- Design of a novel transistor level OTA topology with digitally controlled gate shaping and feedback.
- A simulation-based comparison of the three topologies that evaluates EMI performance and efficiency.

1.4 Thesis Outline

The remainder of this thesis is organized as follows:

Chapter 2 presents the theoretical foundation that should help understand the design challenges. It includes detailed information about the gate charge process and Miller effect, physical properties of MOSFET and general gate driving operation.

Chapter 3 includes a detailed design and analysis of three topologies.

Chapter 4 includes a comparison of three topologies based on the results from Chapter 3. The discussion includes design complexity, layout perspectives, power efficiency and trade-offs of each design.

Chapter 5 summarizes the findings of as well as outlines the potential areas of future research.

CHAPTER 2 FUNDAMENTALS OF MOSFET GATE DRIVING

2.1 The Power MOSFET as a Load

From the gate driver's perspective, the MOSFET is not an ideal switch but rather a non-linear capacitive load which requires a significant amount of transient current. In order to model this behavior it is necessary to step away from the regular capacitance analysis and use the Gate charge term Qg.

$$Q_{gate} = C_{gate} \cdot V_{drv} = \int_0^t I_{gate}\,\mathrm{d}t \tag{2.1}$$

$$t = Q_{gate}/I_{gate} \tag{2.2}$$

2.1.1 Parasitic Capacitances

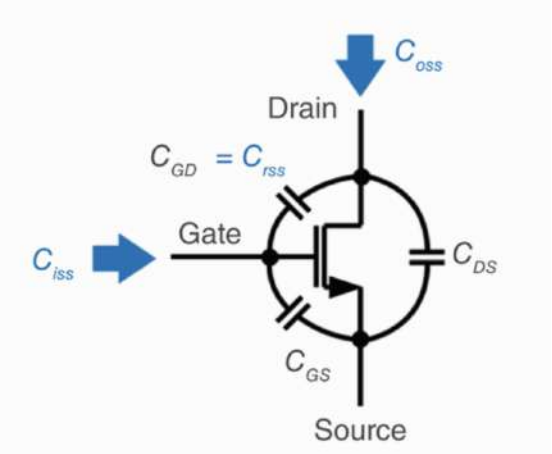


Figure 2.1 – Parasitic capacitances in a MOSFET [3, p. 60]

According to the physical structure of a MOSFET, there are three major parasitic capacitances:

- **Gate-to-Source Capacitance** (next Cgs) is the overlap of the gate electrode with the source and the channel region.
- **Gate-to-Drain Capacitance** (also known as Miller Capacitance, next Cgd) is the overlap of gate with drift region. This capacitance strongly depends on drain-source voltage (next Vds) and is highly non-linear.

- **Drain-to-Source Capacitance** (next Cds) is the junction capacitance of the intrinsic body diode.

Knowing this, it is possible to combine these capacitances to find the terminal values:

- Input Capacitance Ciss = Cgs + Cgd
- Output Capacitance Coss = Cds + Cgd
- Feedback (reverse transfer) Capacitance Crss = Cgd

The reason why the gate charge curve is the preferred method of calculation is because Cgd value changes with Vds. Its capacitance is not constant so it cannot be used for calculations.

2.1.2 The Gate Charge Curve Qg

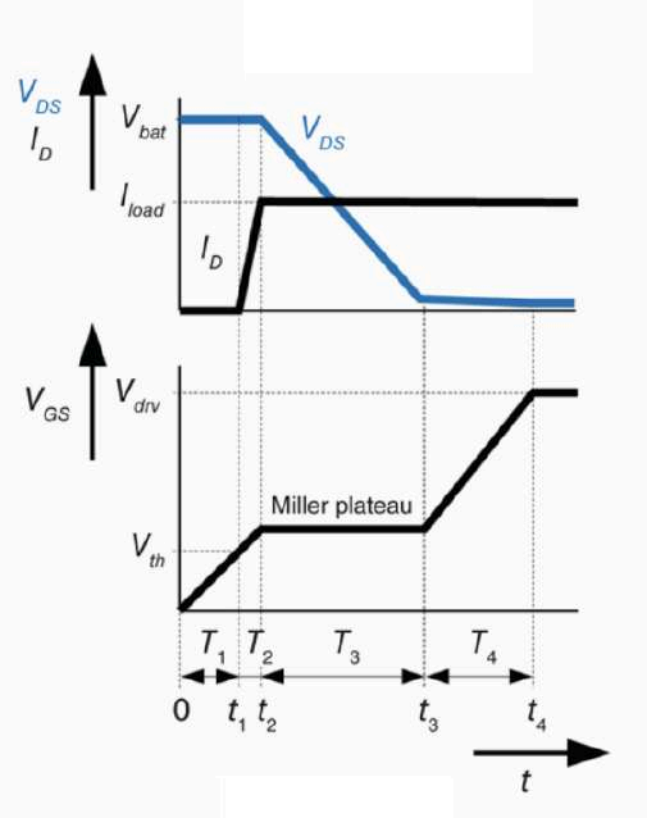


Figure 2.2 – MOSFET Turn-on switching behavior for inductive load [3, p. 65]

The plot on Figure 2.2 shows the total charge injected into the gate Qg versus gate-source voltage Vgs. The curve itself has three distinct regions which define the MOSFET's turn on state.

- **Qgs (gate-source) charge.** This part of the curve shows the initial phase of charging with Vgs rising from 0V to Vth (threshold). Until this point the device is in cutoff so ideally no drain current Id flows. Once Vth is hit, there is the beginning of channel formation with Vgs rising to Vpl and Id rapidly increasing until it hits the load current limit. Vds still remains clamped at Vdd (supply rail). Cgs is charged.
- **Qgd (gate-drain) charge.** This part corresponds to the horizontal part of Vgs known as Miller plateau. Here Vgs remains constant despite current injection. Vds drops significantly while Id remains at a stable rate until the end of the charging cycle. This part of the Qg curve is the primary metric of dV/dt (voltage transient speeds) and switching losses.
- **Qod (overdrive) charge**. The Vgs voltage starts rising from the plateau to its final driver voltage Vdrv as Vgs has dropped to its on-state value Rds-on. This charge effectively reduces Rds-on to its lowest possible value and lowers conduction losses.

This formula shows the total amount of charge required for every charging part of switching cycle:

$$Qg - total = Qgs + Qds + Qod \tag{2.3}$$

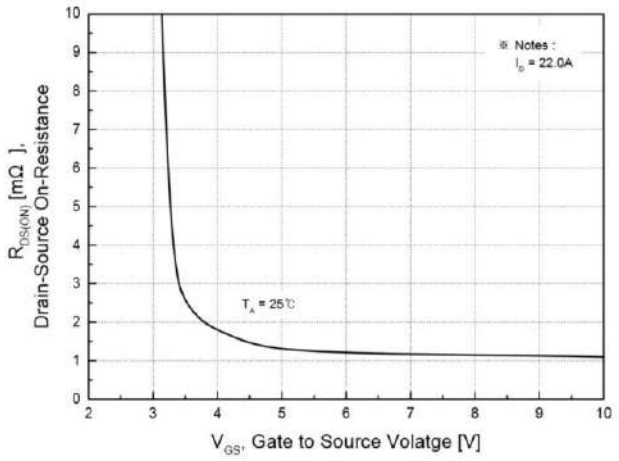


Figure 2.3 – Rds-on versus Vgs relationship [5]

2.1.3 The Miller Plateau and its role in voltage switching and EMI generation.

If the Qg curve shows MOSFET charging process, the Miller plateau is the place where the dynamics of voltage switching process is visible. The plateau is a part of Vgs charging curve that remains flat despite pouring current into the gate. Its formation is caused by negative feedback through gate-drain capacitance Cgd, also called Miller capacitance. At the moment MOSFET turns on, Vds begins to rapidly fall from Vdd to 0. The voltage change across Cgd requires large amounts of displacement current.

$$I = C \cdot dV/dt \tag{2.4}$$

This feedback path (Cgd current path) becomes a short for the gate driver. To support the falling Vds voltage, all current from the driver is forwarded to Cgd leaving no current to raise Vgs. In other words, the falling Vds couples back through Cgd to the gate. Since capacitors resist changes in voltage difference, the falling drain pulls the gate voltage down with it. The more the driver tries pulling the gate up the more the falling drain is pulling the gate down.

During Miller plateau phase, the gate driver loses any control over Vgs. However, it gains control over Vds slew rate. This fundamental capacitor equation defines the relation between speed of Vds falling and gate driver current.

$$\frac{dV_{DS}}{dt} \approx \frac{I_{drv}}{C_{gd}} \tag{2.5}$$

This equation confirms the idea that by shaping the gate Idrv current it is possible to control the switching speed.

Simply put, Miller plateau is a high frequency noise generator. The EMI it produces can be divided into two categories, electric field noise and magnetic field noise.

The dV/dt Generator or electric field noise. The fast drop of Vds voltage turns the drain terminal into a broadcasting antenna. The changing electric field couples through stray capacitance to the chassis ground. Cstray can often be found between transistor and heatsink. Cstray capacitance creates common mode noise currents which flow outside the intended circuit path

$$I_{CM_noise} = C_{stray} \cdot \frac{dV_{DS}}{dt} \tag{2.6}$$

This type of noise is the most difficult to filter and is the main cause of regulatory failures. Since the driver current sets dV/dt, by reducing the driver strength during the Miller plateau phase, it is possible to directly affect the noise.

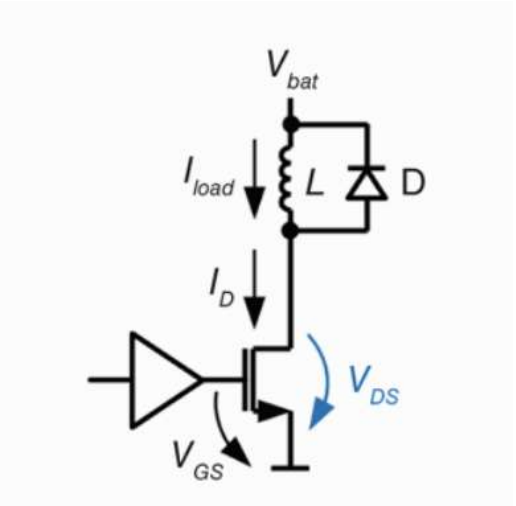


Figure 2.4 – MOSFET load configuration [3, p. 65]

di/dt Generator or magnetic field noise. To better understand the origin of this noise, consider the load configuration from Figure 2.4. There are rapid changes in current before the beginning and after the end of the MIller plateau.

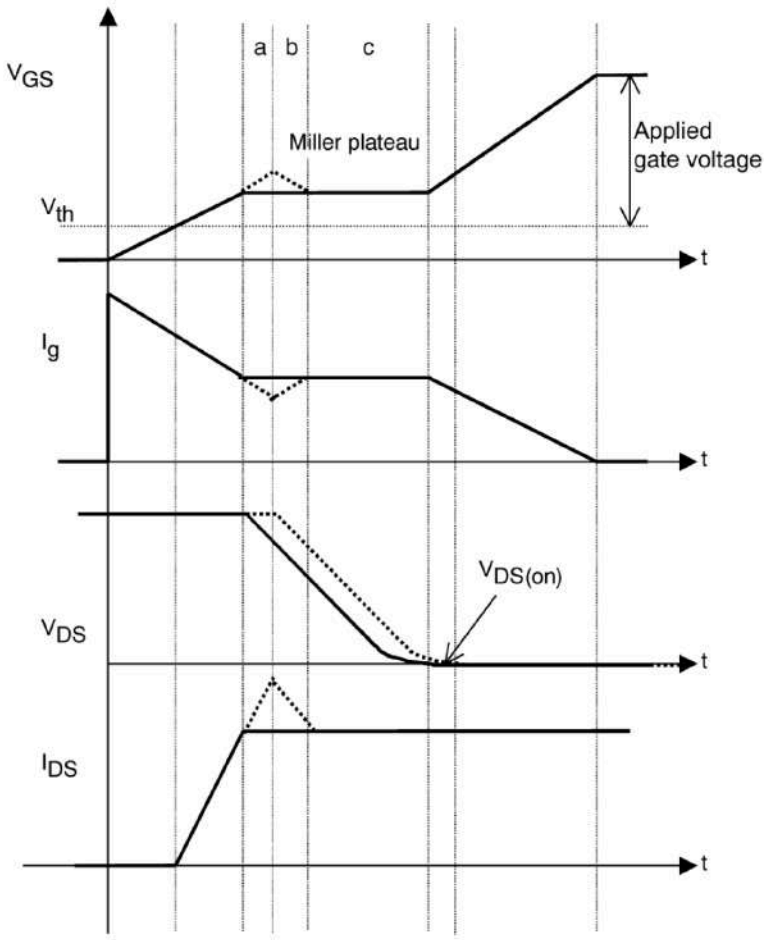


Figure 2.5 – Turn-on waveform for a typical MOSFET in a buck converter [6]

The entry (right before the plateau starts) is the most aggressive ringing event. Ids quickly goes up from 0 current to the max. At the moment Ids hits the max current value it abruptly stops rising, as the inductive load clamps the current. In other words, it goes from positive di/dt to 0 in a short period of time. Such a sudden stop in di/dt is a shock for parasitic inductances in drain/source paths. The inductance is trying to keep the current constant (according to Lenz's Law [7], an inductor opposes any change in current), gets an overshoot and the circuit snaps back forcing Cstray and Lstray to oscillate. Such ringing sits on top of voltage during entering plateau.

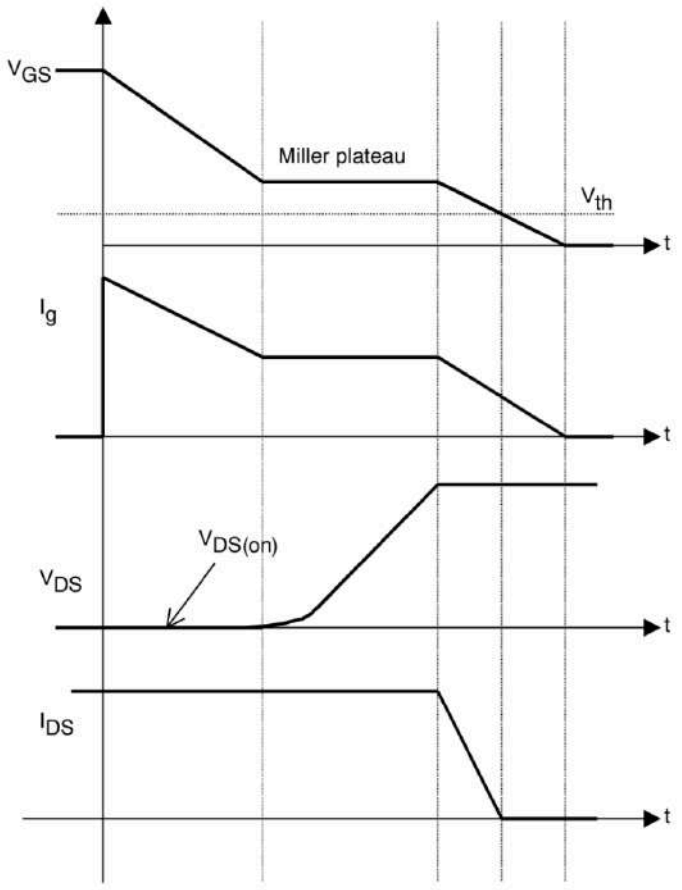


Figure 2.6 – Turn-off waveform for a typical MOSFET in a buck converter [6]

The reverse (negative di/dt) happens at the turn-off event. If the turn-on event generates the noise via injection of current, the turn-off event generates noise via interruption of current. This happens right after the Vgs passes the Miller Plateau and Vds rises back to Vdd. This is the moment when the MOSFET channel is cut-off and the Ids current collapses from full load to 0 almost instantly. This creates a negative di/dt event of high magnitude and collapses the magnetic field stored in parasitic loop inductance Lstray. Once again, According to Lenz's Law[7], the collapsing field induces a large voltage spike across the inductance to oppose the change.

$$V_{spike} = -L_{stray} \cdot \frac{di}{dt} \tag{2.7}$$

This spike is a significant overshoot on the drain node that often exceeds the supply voltage. This overshoot excites the parasitic LC, which results in a high-frequency voltage ringing that radiates differential mode noise. Minimizing the loop inductance is important for preventing the turn-off overshoot from exceeding the MOSFET's breakdown voltage.

While the parasitic elements cannot be eliminated (only reduced by decoupling caps, clever routing of ground planes etc.), the ringing may be suppressed at the source. This brings once again to the importance of controlling slew rate of VGS at the Miller Plateau as this can reduce the di/dt and dV/dt excitation energy delivered to the parasitic LC tank. Since it prevents the oscillation from the start, it effectively neutralizes the negative impact of parasitics without any changes in external hardware.

2.1.4 Spectral Implications

The switching event from a DSP perspective is a trapezoid pulse. The harmonic of the pulse is bound to two corner frequencies. The roll-off of high frequency noise is determined by the second corner frequency and is inversely

proportional to the switching transition time. Shaping the gate driver's pulse directly attenuates fc2 [8].

$$f_{c2} = \frac{1}{\pi t_r} \tag{2.8}$$

A tradeoff between high switching losses and high EMI is all about controlling the plateau.

2.2 Purpose of Gate Drivers

The control algorithms in modern power electronics are mostly executed by low voltage digital processors ranging from simplest microcontrollers up to FPGAs. These devices excel at complex calculations, logic and signal processing but their output stages are designed for signal transmission only, therefore, they are lacking the capabilities to drive heavy loads.

As previously established during the gate charge analysis, the input impedance of the power MOSFET has capacitive nature. The transistor switching speed is directly impacted by the speed at which it is able to deliver and remove the charge to/from gate capacitance as confirmed by I = dQ/dt. Standard GPIO pins are generally defined by high output impedance thus their capabilities of driving loads/sinking current is limited to mA range.

As an example, according datasheet of the popular Xilinx Zynq-7020 FPGA, Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks[9] while the chosen Power mosfet requires up to 600mA of gate current for effective switching.

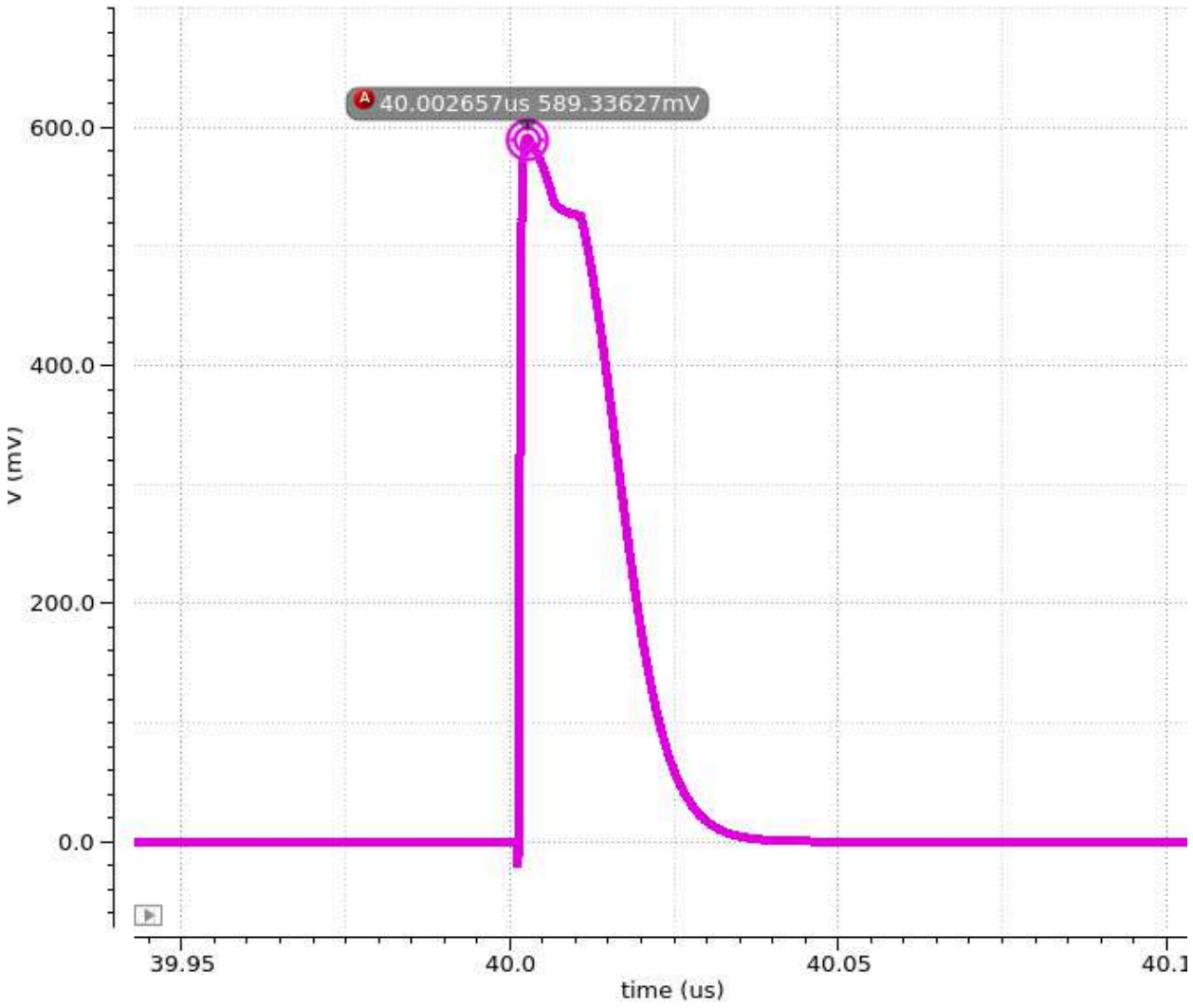


Figure 2.7 – Simulated gate current of a charging event of IAUCN04S7L028 MOSFET

Given the required current, it becomes apparent that a direct connection is functionally insufficient and the gate driver is the necessary mediator between control logic and high power switching domain. The gate driver functions as a current buffer which means it presents high-impedance input to minimize loading on the controller. It also provides low-impedance output so it is able to deliver large amounts of current that is necessary to efficiently charge and discharge the MOSFET gate capacitance. Another important function that gate drivers serve is voltage shifting. The current trend of improving efficiency and power saving leads to lowering the system voltage. Throughout the last decade, the general microcontroller voltage has dropped from 5V to 1.8-1.3V. According to the

datasheet of the selected power MOSFET IAUCN04S7L028 [10], it requires at least 4.5V Vgs (it can accept up to 16V) to maintain proper functioning like minimizing Rds-on and fully enhancing the channel. Even though the microcontroller might be able to reach the MOSFET threshold voltage, it is highly unlikely it will be able to force the mosfet even into a deep triode mode. The MOSFET operation with gate voltage near threshold level results in an increased channel resistance which equals high conduction losses. The gate driver translates this low-voltage GPIO signal from a controller into a drive signal of high enough amplitude that satisfies the optimal saturation characteristics of the power MOSFET and ensures optimal conduction losses.

2.3 Fundamental Design Challenges

2.3.1 Cross-Conduction (Shoot-Through)

Cross conduction is one of the biggest challenges as the push-pull configuration will be used as the output stage for every topology. Push-pull typically consists of high side and low side (pMOS and nMOS). The task of the high side is to source the current from Vdd to charge the gate while the task of the low side is to sink the current to discharge the gate to Vss. Ideally, they should be operating in a complementary fashion (One turns off only after another turns on). However, the real-world transistors show inherent propagation delay between the moment the control signal arrives at the gate and the moment the channel is completely formed or collapsed. Therefore, there is a transient overlap where both high and low sides are partially on at the same time. This creates a low resistance path from Vdd to Vss and this path entity bypasses the load. This phenomenon is called cross-conduction [21].

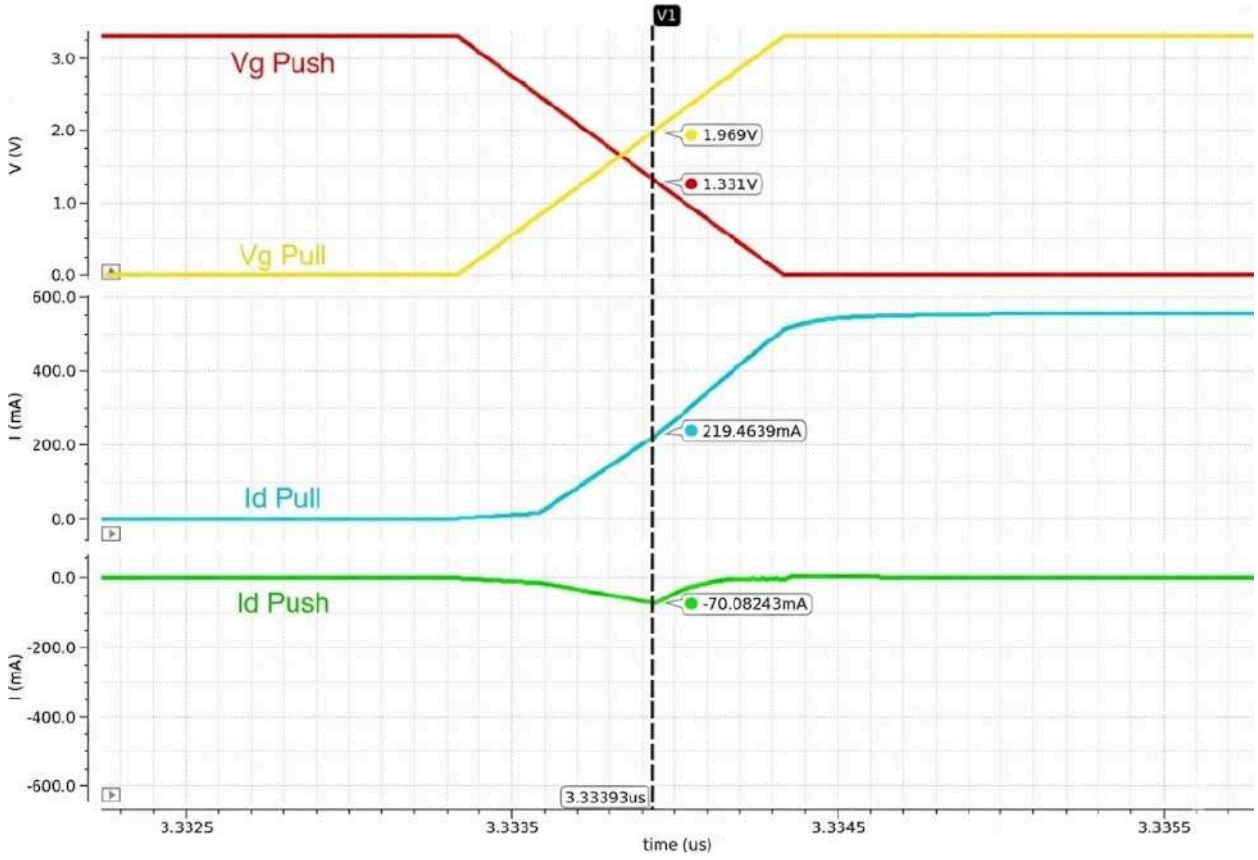


Figure 2.8 – Gate voltages and currents of push-pull showing cross-conduction.

The only limiting factor for current during cross-conduction is combined Rds-on of both MOSFETs and power supply impedance (neglected here).

$$I_{cc} = \frac{V_{DD} - V_{SS}}{R_{on,High} + R_{on,Low}} \tag{2.9}$$

MOSFETs are designed to have a low Rds-on value (typically < 1/Omega). The cross-conduction may exceed the safe ratings by an order of magnitude leading to the supply rail collapse or thermal destruction. Supply rail collapse happens when a massive current demand causes the supply voltage to droop. This has the potential of interfering with sensitive circuits that share the same power rail, for example, resetting the microcontroller. Thermal destruction happens when the current rise causes I^2R heating of the gate driver's die. This may result in thermal runaway and circuit failure.

The solution to cross-conduction is introducing a dead-time circuit like Break-Before-Make or using asymmetrical sizing (which will be discussed in the next chapter).

2.3.2 Power Losses

An important metric of any power converter is the total energy dissipated within a MOSFET or power losses. They can be roughly divided into two categories such as conduction and switching losses.

Conduction Losses (Pcond) happen when the MOSFET is fully on (fully enhanced). The behavior of the device is comparable to a linear resistor so the key parameter here is transistor Rds-on. This metric primarily depends on the die size of the MOSFET, however, as stated in 2.2, the gate driver plays a crucial role in minimizing it by setting a Vgs of a high enough level to make sure the channel is fully enhanced, minimizing the Rds-on. If the channel is only partially enhanced, this increases thermal dissipation as Rds-on increases. The equation is:

$$P_{cond} = I_{rms}^2 \cdot R_{DS(on)} \tag{2.10}$$

Switching Losses (Psw) happen during transition between on/off states. This metric involves presence of both Id and Vds at the same time. Such overlap creates an instantaneous power spike. Important parameters here are the on/off transition time defined by Miller capacitance and switching frequency. The equation is

$$P_{sw} \approx \frac{1}{2} V_{DS} \cdot I_D \cdot (t_{on} + t_{off}) \cdot f_{sw} \tag{2.11}$$

where

$$t_{on} \approx t_{plateau} = \frac{Q_{gd}}{I_{gate}} \tag{2.12}$$

The cost of EMI reduction represents the classic engineering conflict. EMI reduction inevitably increases switching losses [16]. To be more specific, The gate driver has to source high Igate to minimize transition time and maximize efficiency. Minimizing transition time increases dV/dt and di/dt which in its term maximizes EMI [17]. The engineer's task here is not to minimize some aspect at the expense of another but rather seek for an optimal balance with the transition time slow enough to meet EMI requirements but fast enough to stay efficient.

MOSFET Output Capacitance Loss (Poss). Coss charges to the bus voltage while the device is in the off state. Once the device turns on, the energy stored as

$$\frac{1}{2} C_{oss} V^2 \tag{2.13}$$

is discharged and dissipated as heat. The driver has no control over the fixed amount of energy losses and the speed at which the discharge occurs has a direct impact on di/dt that influences EMI.

Gate Driver Losses (Pdrive). Even though the focus is mainly on losses of the power MOSFET, the gate driver also consumes some amount of energy. These

losses include static consumption, like bias circuitry in OTA and the power dissipated by push-pull pair that charges/discharges Vgate of power MOSFET

$$P_{drive} \approx Q_G \cdot V_{drv} \cdot f_{sw} \tag{2.14}$$

Since it is quite troublesome to isolate specific losses on the testbenches, this work utilizes the 'sum of losses' metric. This consists of the sum of power used by load versus total power consumed by the circuit.

$$P_{tot} = P_{load} + P_{MOSFET} + P_{driver} + P_{passive} \tag{2.15}$$

This equation consists of:

P_{load} Power delivered to the load of the boost converter.

P_{driver} **(**$P1 + P2$**):** Power used by gate driver circuit + push-pull output stage

P_{MOSFET} **(**$P3$**):** Power used by the MOSFET

$P_{passive}$**:** Power used by inductor and diode in the boost converter, however, neglected at calculation since ideal components are used.

Total system efficiency is calculated with this equation:

$$\eta = \frac{P_{load}}{P_{load} + P_{MOSFET} + P_{driver}} \times 100\% \tag{2.16}$$

2.3.3 Parasitics

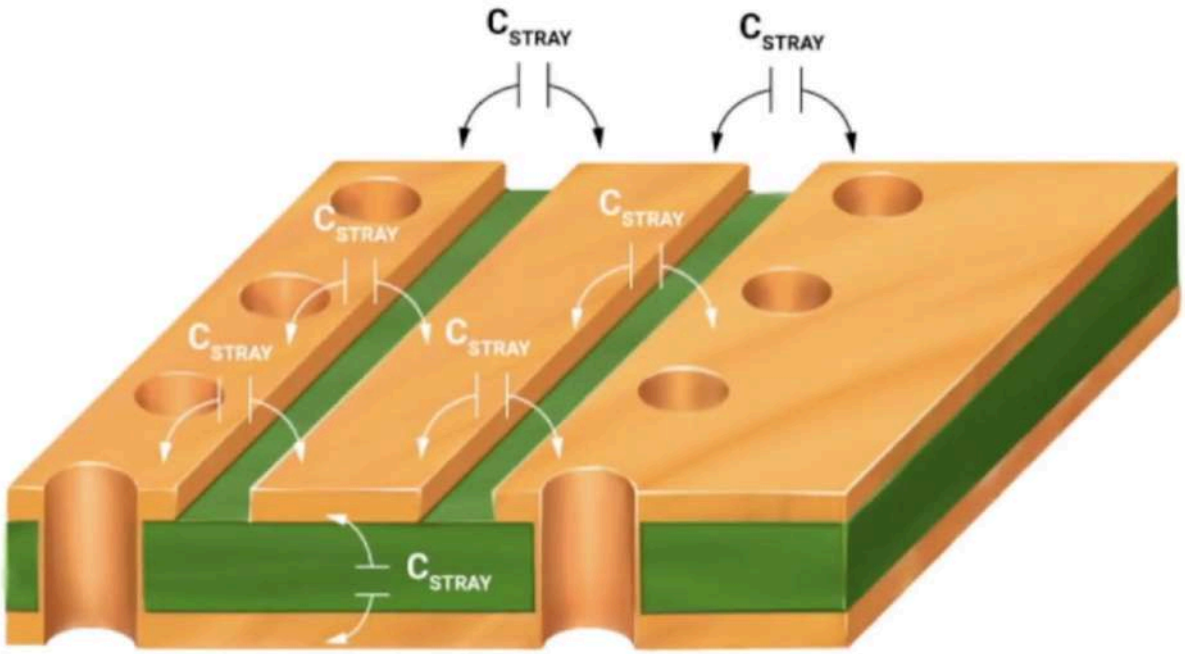


Figure 2.9 – PCB Cstray parasitics [11]

Unlike the schematic with ideal components and zero-impedance wires, real devices possess intrinsic parasitic properties. Every bond wire, component lead or pcb trace has parasitic resistance, inductance and capacitance. They may be harmless at lower frequencies, but they may significantly alter the circuit behavior in high-frequency domain

The most important parasitic in power switching sequence is stray inductance (Lstray) as it opposes the changes in current flow [18]. This inductance can be roughly divided into two loops, the gate loop (Lgate) and power loop (Lpower).

Lgate is formed by the entire control circuit loop: extending from the driver output, through the gate trace to the MOSFET, and returning from the MOSFET source back to the driver ground. The di/dt in gate current leads to voltage drops across the loop. This reduces the voltage that actually gets to the die and the switching speed is also reduced, occasionally leading to oscillations. Lpower is formed by a path from the power MOSFET and load (which may include a diode or output capacitor). This path experiences a full load current transition during the switching process. The rapid change creates a voltage spike (according to Faraday's law)

$$V_{spike} = -L_{power} \cdot \frac{di_D}{dt} \tag{2.17}$$

This Vspike adds up to the bus voltage and the total voltage overshoot on the node may exceed the breakdown voltage and cause avalanche breakdown.

Another important parasitic is stray capacitance (Cstray) which includes the internal mosfet capacitance and capacitance between pcb traces and chassis ground. Together with parasitic inductance these capacitances form an LC tank circuit. At the moment the MOSFET switches, a fast energy impulse excites the LC tank which starts resonating at some natural frequency.

$$f_{res} = \frac{1}{2\pi\sqrt{L_{stray} \cdot C_{par}}} \tag{2.18}$$

This decaying sinusoidal wave superimposed on the switching edge or simply oscillation is called voltage ringing, which can turn the pcb trace into a broadcasting antenna. This oscillation is typically falling into the 30Mhz-300Mhz range, which is strictly regulated by EMC standards. The ringing duration is determined by internal resistance of components and the parasitic resistance of the traces.

Minimizing EMI does not only slow the switching speed or make the circuit more efficient. It also minimizes stray inductance to push resonant frequency higher so it has less energy and reduced magnitude of the initial voltage spike.

CHAPTER 3 DESIGN AND ANALYSIS OF GATE DRIVER TOPOLOGIES

3.1 The Test Load: A Boost Converter Power Stage

In order to evaluate the proposed gate drivers, a universal testbench needs to be established. Rather than simply using an idealized capacitive load of 2.4nF (gate capacitance of the chosen power MOSFET) the topologies should be tested in a hard-switching environment that resembles a real-world power converter. For this purpose, a simplified asynchronous Boost Converter [19] that is used to step up the dc voltages will be used.

Schematic Configuration:

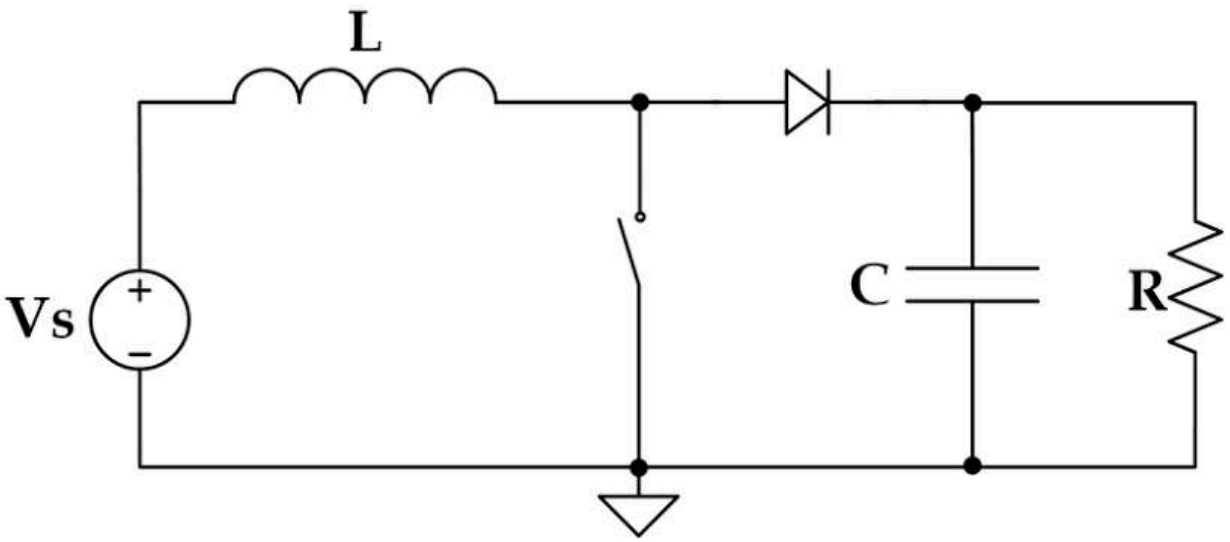


Figure 3.1 – Asynchronous boost converter [12, p. 24]

This testbench consists of a power inductor, an ideal diode, power MOSFET used as a switch (SPICE model), ideal capacitor and a load resistor.

Component Specifications:

Power MOSFET: A high-performance N-channel power mosfet suitable for automotive applications.

- **Model:** Infineon IAUCN04S7L028

- **Total Gate Charge (Q_G):** $\approx 100\text{nC}$ (at $V_{GS} = 10\text{V}$)
- **Input Capacitance (C_{iss}):** $\approx 2.4\text{nF}$

Power Inductor (L): An off-the-shelf power inductor modeled to provide realistic saturation characteristics.

- **Model:** Coilcraft PA6331-AL
- **Inductance:** $15\mu\text{H}$
- **Saturation Current (I_{sat}):** 20A

Diode (D): An ideal diode model was used to isolate the switching characteristics of the MOSFET from diode reverse-recovery effects.

Load: ($R = 50\Omega$) Ideal resistor model was used so the converter operates in a Continuous Conduction Mode during the switching cycles.

Capacitor: ($C = 10p$): An ideal capacitor model is parallel with the load. Unlike real world applications where the capacitor is massive and provides ripple reduction and energy hold up at turn off events, this tiny capacitor is placed to simulate the parasitic node capacitance.

Such testbench forces the gate driver to not only manage the charging of Vgate of power MOSFET but also the Miller effect caused by fast drain voltage transitions inductive kickback during turn off event. All simulations for this paper were performed using this configuration.

3.2 The Basic Push-Pull Driver

3.2.1 The CMOS Inverter Output Stage

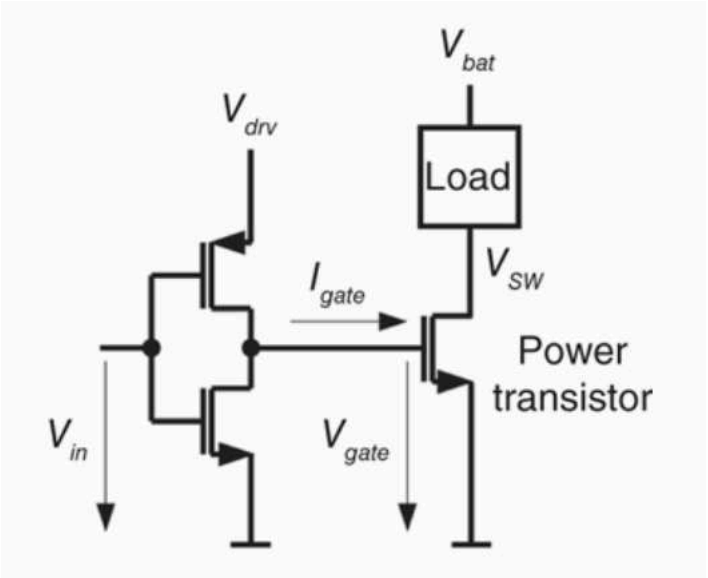


Figure 3.2 – The CMOS Inverter Output Stage [3, p. 262]

The basic topology that will be a baseline for comparison will be the conventional CMOS push-pull stage (sometimes called totem-pole). This topology is a common design choice because of its simplicity, ability to swing rail-to-rail and near zero static power consumption. Such a circuit consists of a Pmos MOSFET with a source connected to Vdd, gate to input and drain to output. Nmos Has gate tied to input, drain to output and source to ground reference or Vss [14]. The circuit operates as a bi-directional current switch whose primary function as a gate driver is impedance transformation. The microcontroller's logic signal source has limited current driving capability and high output impedance. The push-pull on the contrary provides high impedance capacitive load to the source and low impedance output to power MOSFET. Such configuration allows to source and sink transient currents that are necessary for charging and discharging MOSFET gate capacitance [15].

The operation of the push-pull gate driver occurs in two distinct phases: turn-on (charging) and turn-off (discharging).

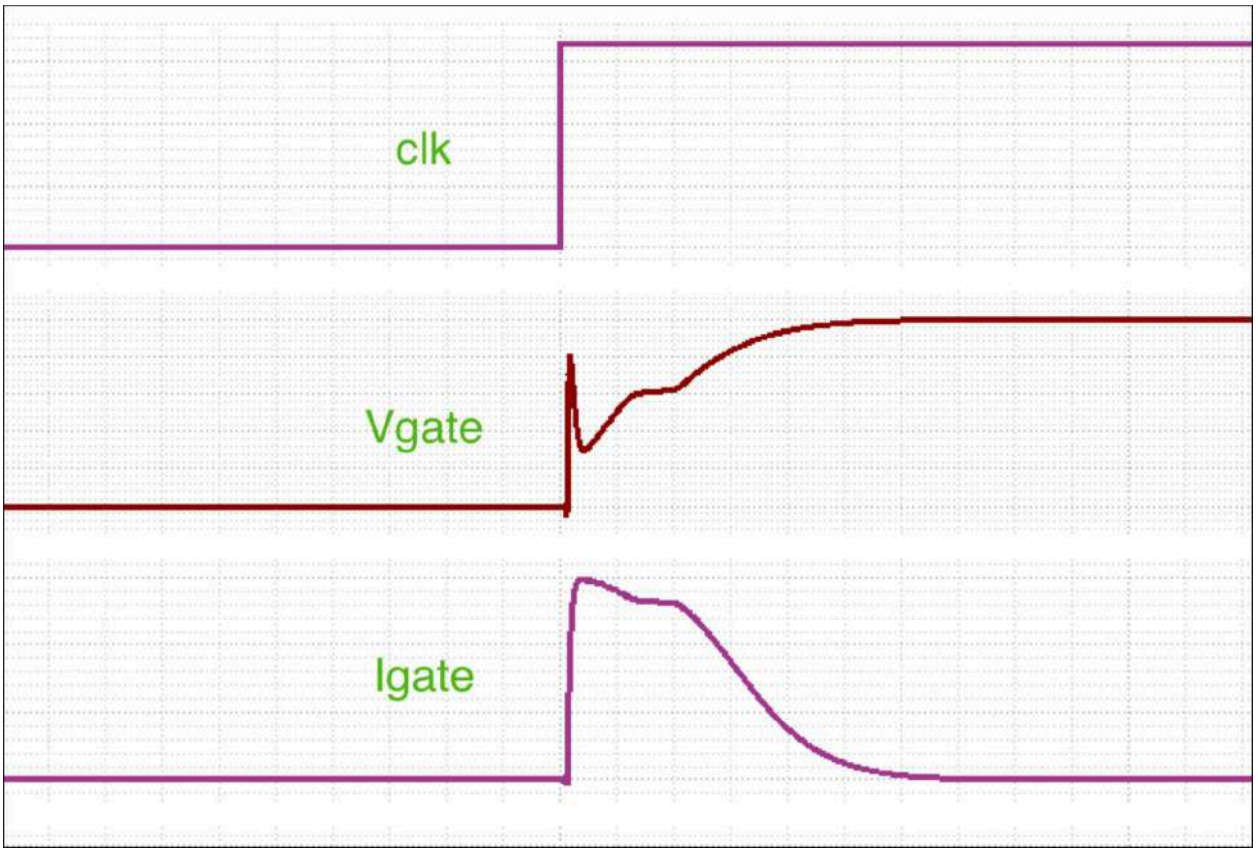


Figure 3.3 – The charging phase of a push-pull gate driver.

When input receives a logic low signal, Nmos enters the cut-off mode. Pmos enters saturation mode and creates a conduction path from Vdd to the gate of power MOSFET. The current flows through this path and charges Ciss input capacitance. The rate of turn-on speed of power MOSFET as well as rate of voltage rise is limited by total gate charge and Rds-on.

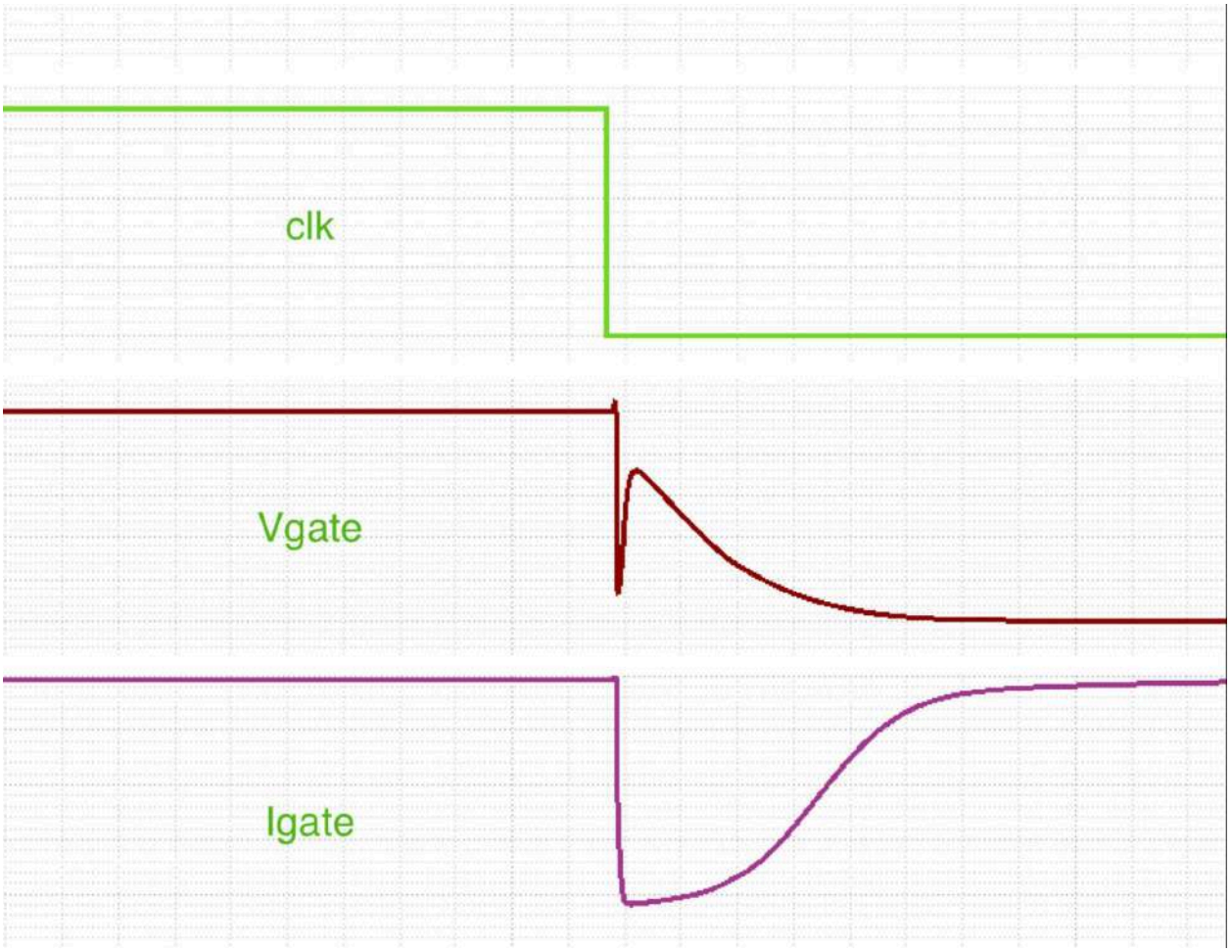


Figure 3.4 – The discharging phase of a push-pull gate driver.

Similarly to the charging, when input receives a logic high signal, Pmos enters the cut-off mode and Nmos turns on into saturation. It creates a low resistance path from Vgate of power MOSFET to Vss. All the charge stored on the gate capacitor is shunted to Vss. This turns off the device.

The switching speed of the baseline topology is determined by supply voltage and physical sizes of the transistors. The downside of this is once the circuit is fabricated there is no way to change the driver strength. Such a circuit lacks any kind of adjustment or feedback so it simply applies all the voltage it has to the load. Such uncontrolled behavior of the circuit provides the fastest possible switching time at the expense of fast slewing rates and as a result the most aggressive EMI.

3.2.2 The Limitations of a Single Stage

The easiest implementation of such a gate driver is to size it to deliver the required current. Such an approach leads to another fundamental issue of this topology. The driver MOSFET's W/L ratio should be > 1000 in order to drive input capacitance of 2.4nF fast enough. While it is possible to drive the load, push-pull's own input capacitance becomes enormous for a weak microcontroller's logic to drive it. According to the equation,

$$\tau = R_{source} \times C_{load} \tag{3.1}$$

and since Cload of MOSFET with W/L > 1000 is too big, it may take a lot of time to charge it. The PWM signal will look like a slow ramp instead of a sharp square wave. Such a fan-out problem requires a multi-stage solution. Additionally, a regular push-pull has the cross-conduction issue (discussed in details in chapter 2). Since these are huge MOSFETs, the cross current during state transitions will be significant. Given that the switching event is even slower because of weak MCU output capabilities, the duration of cross conduction is even longer which can lead to dangerous power dissipation within the driver itself.

3.2.3 The Tapered Buffer

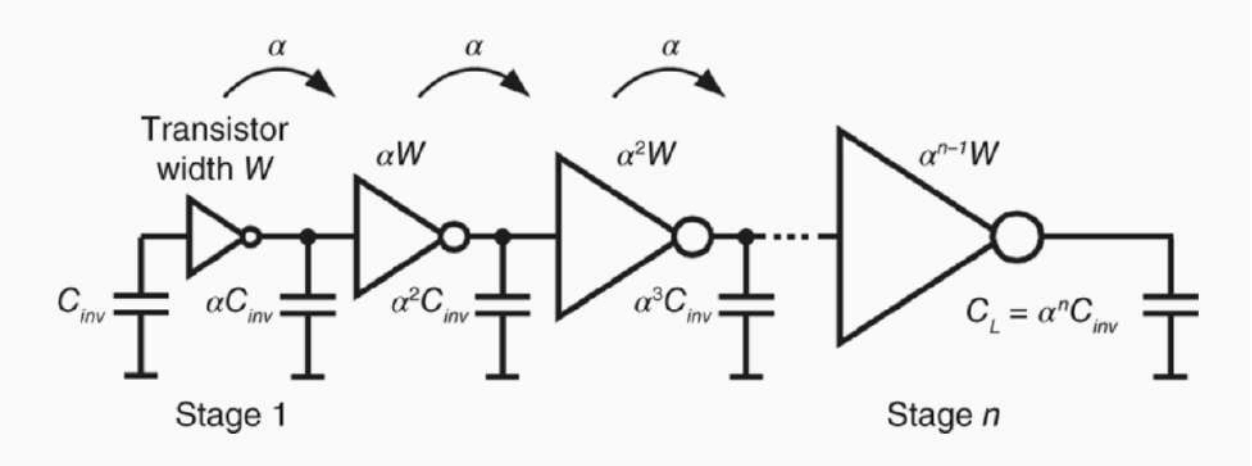


Figure 3.5 – The tapered buffer architecture [3, p. 301]

The solution to this problem of low input capacitance and high output drive strength is the architecture called tapered buffer. It consists of cascade of n inverter stages. Each stage is f times larger (W/L ratio) than the previous one. Such a scaling ensures that each state is capable of driving a load proportional to its

strength. The first stage usually has the minimal size to be a light load for the mcu. It drives the next stage which drives the next stage until reaching the final MOSFET. The effort is distributed across all stages while keeping the minimal propagation delay. The equation 3.2 for the scaling factor (f) shows the relationship between the number of stages (N), load capacitance (C_{load}) and first stage capacitance (C_{in}). A scaling factor of 4 was chosen for this design which resulted in a driver chain of 6 stages.

$$f = \sqrt[N]{\frac{C_{load}}{C_{in}}} \tag{3.2}$$

The physical properties of the silicon require to size Nmos and Pmos asymmetrically to compensate for the hole vs electron mobility. Pmos will be scaled 2.5 times wider than Nmos for the ease of calculation. This ratio should ensure the similar rise and fall times for gate waveform.

The Sizing Calculations (3.3)

From datasheet of IAUCN04S7L028 [10]

$$\text{Input capacitance} \quad C_{\text{iss}} = 1578\,\text{pF}$$
$$\text{Output capacitance} \quad C_{\text{oss}} = 788\,\text{pF}$$
$$\text{Gate charge} \quad Q_g = 24\,\text{nC}$$
$$\text{Rise/Fall time} \quad \Delta t = 40\,\text{ns}$$
$$V_{\text{GS,max}} = 5\,\text{V}$$

From PDK Parameters [13]

$$L_{\text{nMOS,min}} = 0.45\,\mu\text{m}$$
$$k_n = 74.55621302\,\mu\text{A/V}^2$$
$$V_{\text{GSn}} = 3.3\,\text{V}$$
$$V_{\text{thn}} = 0.7\,\text{V}$$

The equations from [3]

$$I_g = \frac{Q_g}{\Delta t}$$

$$I_g = \frac{24\,\mathrm{nC}}{40\,\mathrm{ns}} = 0.60\,\mathrm{A}$$

$$C_{\mathrm{tot}} = C_{\mathrm{iss}} + C_{\mathrm{out}}$$

$$C_{\mathrm{tot}} = 1578\,\mathrm{pF} + 788\,\mathrm{pF} = 2366\,\mathrm{pF}$$

$$R_{\mathrm{on}} = \frac{V_{\mathrm{out,max}}}{I_g}$$

$$R_{\mathrm{on}} = \frac{5\,\mathrm{V}}{0.60\,\mathrm{A}} = 8.33\,\Omega$$

$$V_{\mathrm{ov,n}} = V_{\mathrm{GSn}} - V_{\mathrm{thn}}$$

$$V_{\mathrm{ov,n}} = 3.3\,\mathrm{V} - 0.7\,\mathrm{V} = 2.6\,\mathrm{V}$$

$$W_n = \frac{2I_{D,n}L_n}{K_n V_{\mathrm{ov},n}^2}$$

$$W_n = \frac{2 \cdot 0.60\,\mathrm{A} \cdot 0.45\,\mu\mathrm{m}}{(74.55621302 \times 10^{-6}\,\mathrm{A/V^2}) \cdot (2.6\,\mathrm{V})^2} = 1071.43\,\mu\mathrm{m}$$

$$W_p = \frac{2I_{D,p}L_p}{K_p V_{\mathrm{ov},p}^2}$$

$$W_p = \frac{2 \cdot 0.60\,\mathrm{A} \cdot 0.40\,\mu\mathrm{m}}{(27.34 \times 10^{-6}\,\mathrm{A/V^2}) \cdot (2.65\,\mathrm{V})^2} = 2500.06\,\mu\mathrm{m}$$

$$C_{\mathrm{inv},N} = C_{\mathrm{ox},N}\, L_{\mathrm{in},N}\, W_{\mathrm{in},N}$$

$$C_{\text{inv},N} = 4.82\,\frac{\text{fF}}{\mu\text{m}^2} \cdot 0.45\,\mu\text{m} \cdot 0.9\,\mu\text{m} = 1.950518836\,\text{fF}$$

$$C_{\text{inv},P} = C_{\text{ox},P}\,L_{\text{in},P}\,W_{\text{in},P}$$

$$C_{\text{inv},P} = 4.69\,\frac{\text{fF}}{\mu\text{m}^2} \cdot 0.40\,\mu\text{m} \cdot 2.00\,\mu\text{m} = 3.750133333\,\text{fF}$$

$$C_{\text{inv}} = C_{\text{inv},N} + C_{\text{inv},P}$$

$$C_{\text{inv}} = 1.950518836\,\text{fF} + 3.750133333\,\text{fF} = 5.700652169\,\text{fF}$$

$$C_{\text{gate}} = W_n\,L_{\text{nMOS}}\,C_{\text{ox},N}$$

$$C_{\text{gate}} = 1070\,\mu\text{m} \cdot 0.45\,\mu\text{m} \cdot 4.82\,\frac{\text{fF}}{\mu\text{m}^2} = 2322.63\,\text{fF}$$

$$\frac{C_g}{C_{\text{inv}}} = \frac{C_{\text{gate}}}{C_{\text{inv}}}$$

$$\frac{C_g}{C_{\text{inv}}} = \frac{2318.950171\,\text{fF}}{5.700652169\,\text{fF}} = 406.7868206$$

$$t_{\text{direct}} = t_{\text{apd}}\,\frac{C_{\text{gate}}}{C_{\text{inv}}}$$

$$t_{\text{direct}} = 41\,\text{ps} \cdot 406.7868206 = 16678.25965\,\text{ps} = 16.67825965\,\text{ns}$$

$$\frac{t_{\text{cas}}}{t_{\text{dir}}} = \frac{t_{\text{cas}}}{t_{\text{direct}}}$$

$$\frac{t_{\text{cas}}}{t_{\text{dir}}} = \frac{1.00\,\text{ns}}{16.67825965\,\text{ns}} = 0.05995829429$$

$$\ln\left(\frac{C_{\text{gate}}}{C_{\text{inv}}}\right)$$

$$\ln\left(\frac{2318.950171}{5.700652169}\right) = \ln(406.7868206) = 6.008289266$$

$$\frac{\ln\left(\frac{C_{\text{gate}}}{C_{\text{inv}}}\right)}{\left(\frac{C_{\text{gate}}}{C_{\text{inv}}}\right)}$$

$$\frac{6.008289266}{406.7868206} = 0.01477011781$$

$$n = \frac{\ln\left(\frac{C_{\text{gate}}}{C_{\text{inv}}}\right)}{\ln(\alpha)}$$

$$n = \frac{6.008289266}{\ln(4.00)} = 4.334064564 \quad \Rightarrow \quad n_{\text{selected}} = 4.00$$

Having all the calculations it is possible to estimate the sizes for each stage:

Nmos

$$\text{Stage } 1 = 1.05\,\mu\text{m}$$

$$\text{Stage } 2 = 4.19\,\mu\text{m}$$

$$\text{Stage } 3 = 16.74\,\mu\text{m}$$

$$\text{Stage } 4 = 66.96\,\mu\text{m}$$

$$\text{Stage } 5 = 267.86\,\mu\text{m}$$

$$\text{Stage } 6 = 1071.43\,\mu\text{m}$$

Pmos

$$\text{Stage } 1 = 2.44\,\mu\text{m}$$

$$\text{Stage } 2 = 9.77\,\mu\text{m}$$

$$\text{Stage } 3 = 39.06\,\mu\text{m}$$

$$\text{Stage } 4 = 156.25\,\mu\text{m}$$

$$\text{Stage } 5 = 625.00\,\mu\text{m}$$

$$\text{Stage } 6 = 2500.00\,\mu\text{m}$$

3.2.4 Asymmetrical Sizing

The main goal in designing a standard high-speed buffer chain is minimizing jitter by maintaining equal rise/fall times. Since this is the high power circuit, the focus shifts from jitter to eliminating cross conduction. The cross conduction issue becomes evident from the simulation results below. When the input signal equals roughly half of Vdd (1,6 - 1.7V) both MOSFETs are on at the same time. The push shows around 90mA of cross current that goes from Vdd straight to Vss. The same happens during the pull stage, around 70mA.

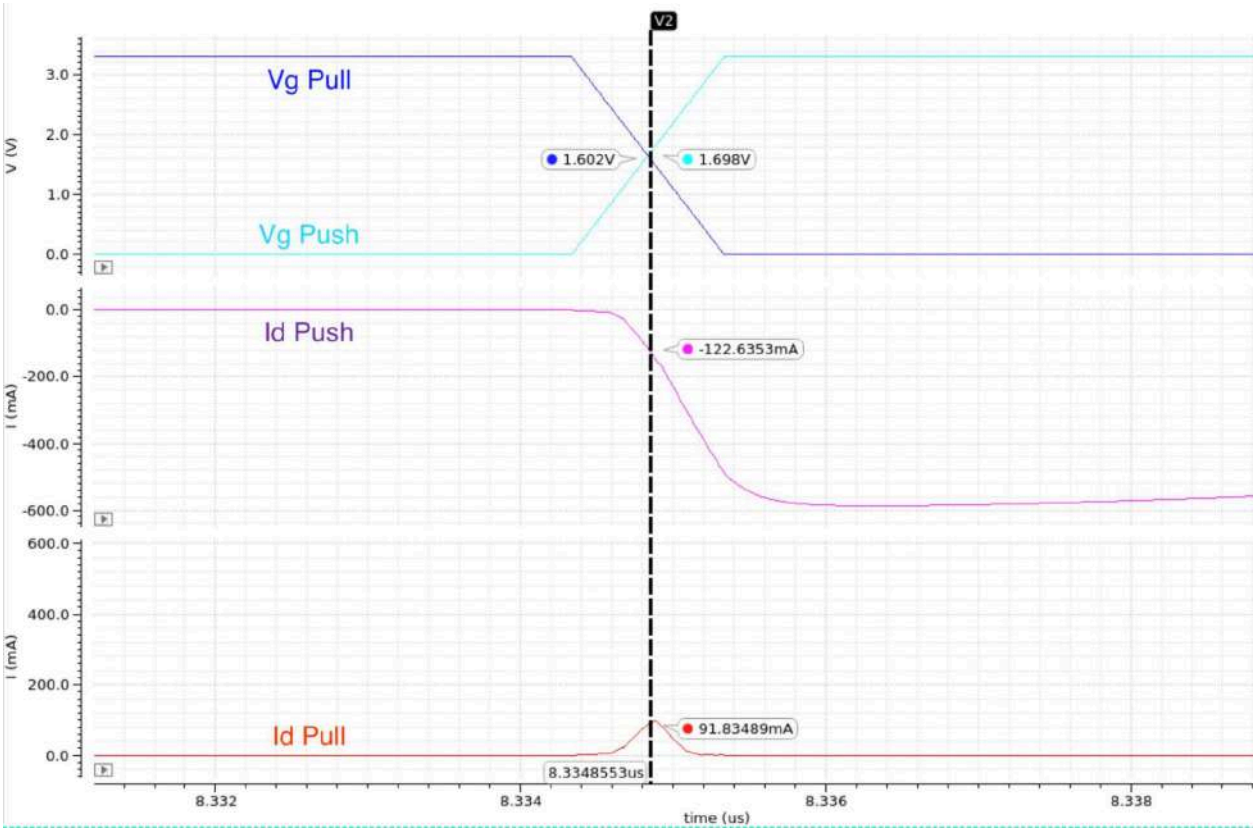


Figure 3.6 – The cross-conduction of 91mA during push stage

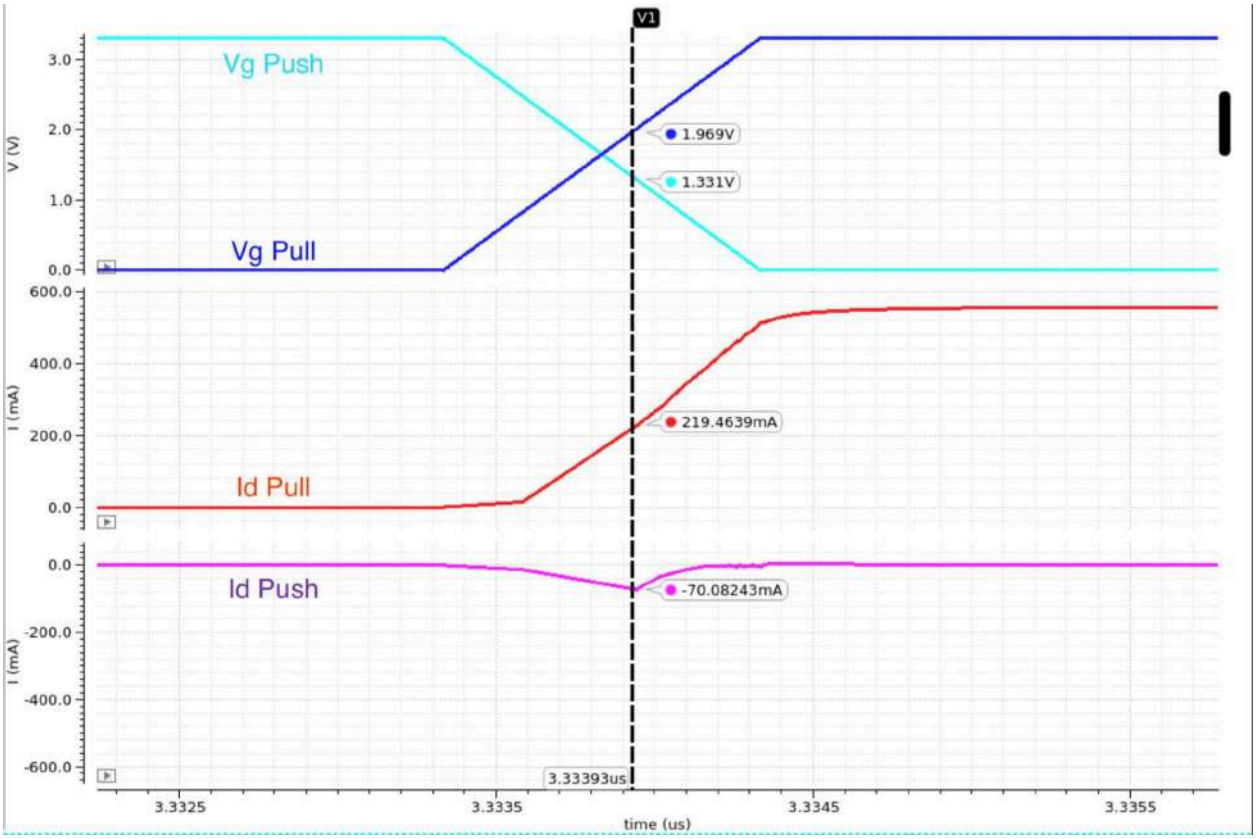


Figure 3.7 – The cross-conduction of 70mA during pull stage

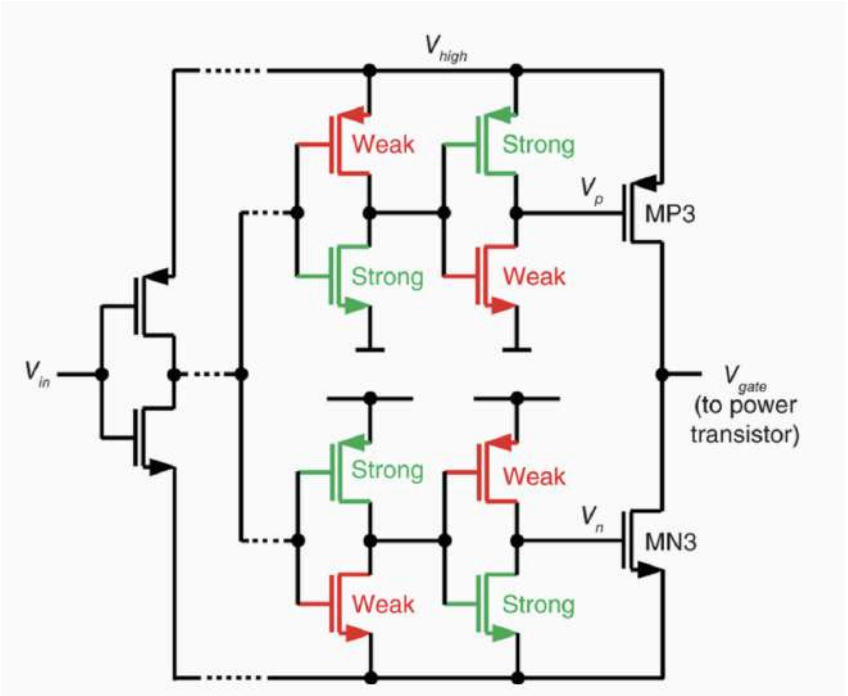


Figure 3.8 – The asymmetrical sizing strategy. Adapted from [3, p. 318].

To address the cross-current issue an asymmetrical sizing strategy will be implemented throughout the tapered chain. The goal is to create a dead time by skewing the switching thresholds of the inverters. It uses two coefficients, weak and strong. The weak coefficient helps delaying the turn on event by decreasing the size of the MOSFETs responsible for next stage turn on. The strong coefficients accelerate the turn off event by increasing the size of the MOSFETs responsible for next stage turn off. This significantly reduces the probability of simultaneous conduction at the expense of slight increase of propagation delay. The asymmetry factor is usually 20-30% but the best value is chosen according to the simulation results. The previously calculated values need to be multiplied by the weak/srtrong coefficient to obtain new sizing values. The initial assumption of 20% worked straight away so below are the exact calculations of each output stage.

Coefficients:

$$\text{Weak} = 0.8$$

$$\text{Strong} = 1.2$$

$$4.19 \cdot \text{Weak} = 3.35 \rightarrow 16.74 \cdot \text{Strong} = 20.09 \rightarrow 66.96 \cdot \text{Weak} = 53.57 \rightarrow 267.86 \cdot \text{Strong} = 321.43$$

$$9.77 \cdot \text{Strong} = 11.72 \rightarrow 39.06 \cdot \text{Weak} = 31.25 \rightarrow 156.25 \cdot \text{Strong} = 187.50 \rightarrow 625.00 \cdot \text{Weak} = 500.00$$

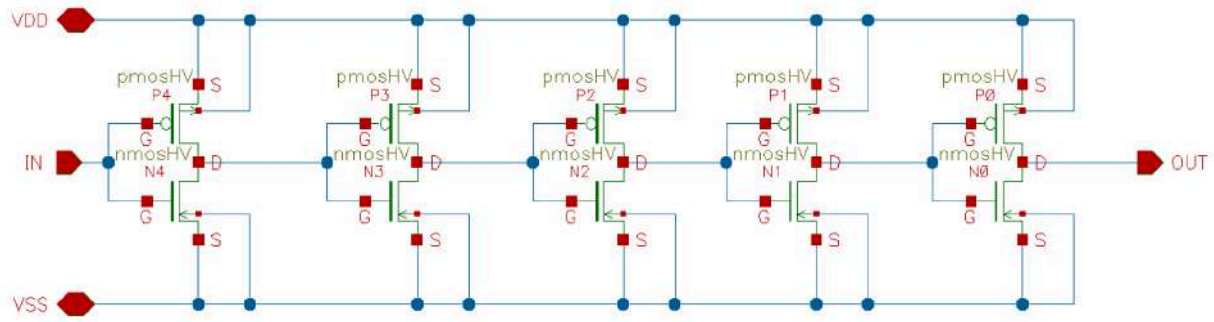


Figure 3.9 – The tapered buffer schematic

3.2.5 The Schematic, Simulation Results and Baseline Characterization

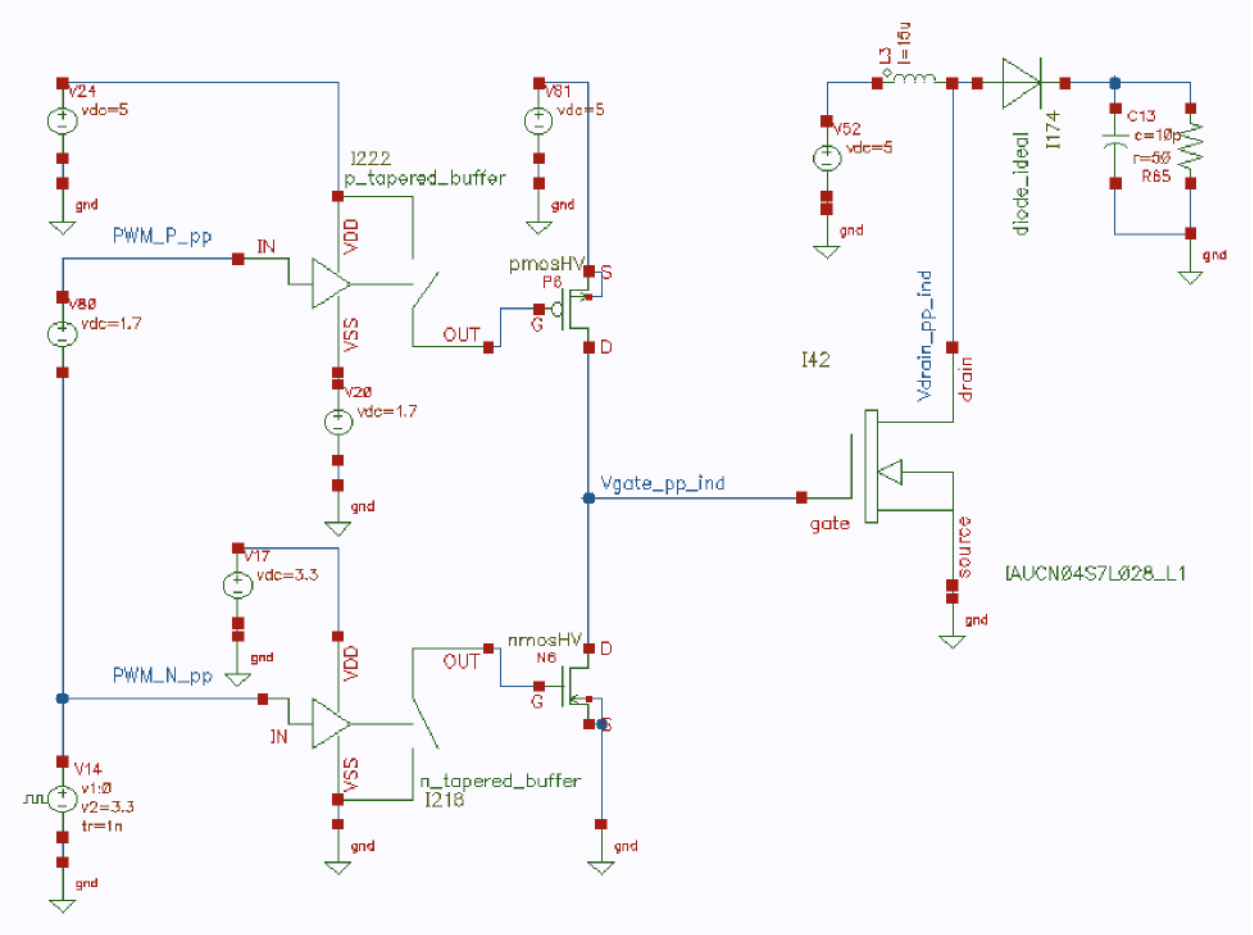


Figure 3.10. Push-pull testbench schematic

In order to evaluate the performance of the asymmetric six-stage tapered push-pull gate driver, the transient simulation with the boost converter as a load was performed.

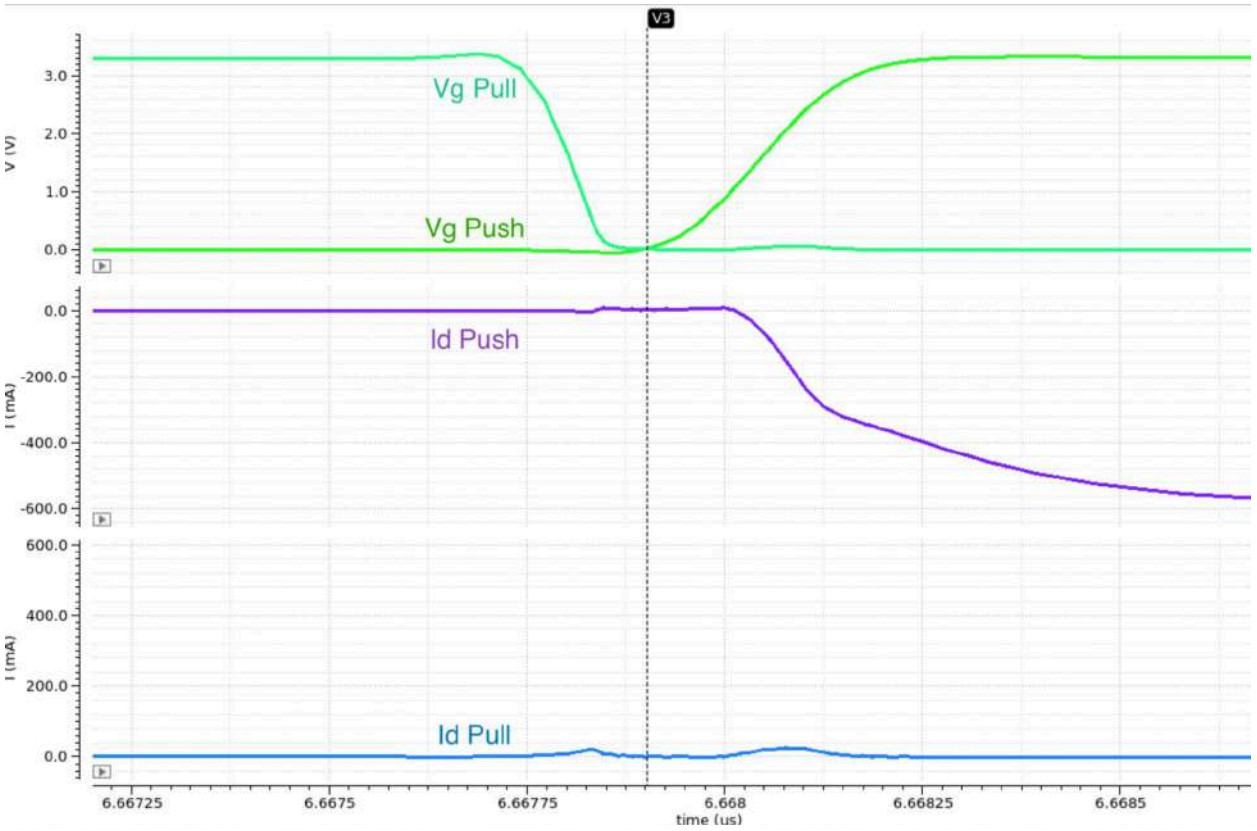


Figure 3.11 – Eliminated cross-conduction during push stage

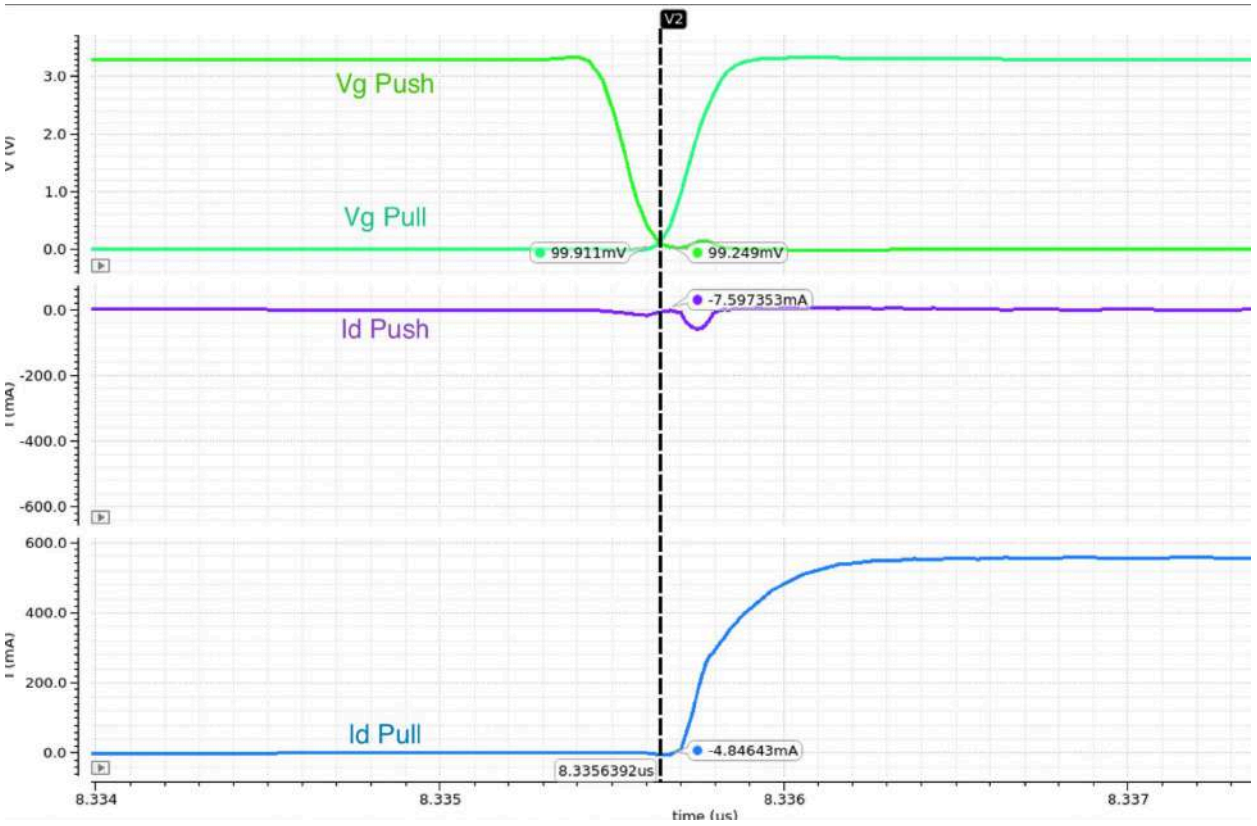


Figure 3.12 – Eliminated cross-conduction during pull stage

The results of the simulation show a clear improvement. The push and pull sequences no longer overlap so there is almost no cross conduction left.

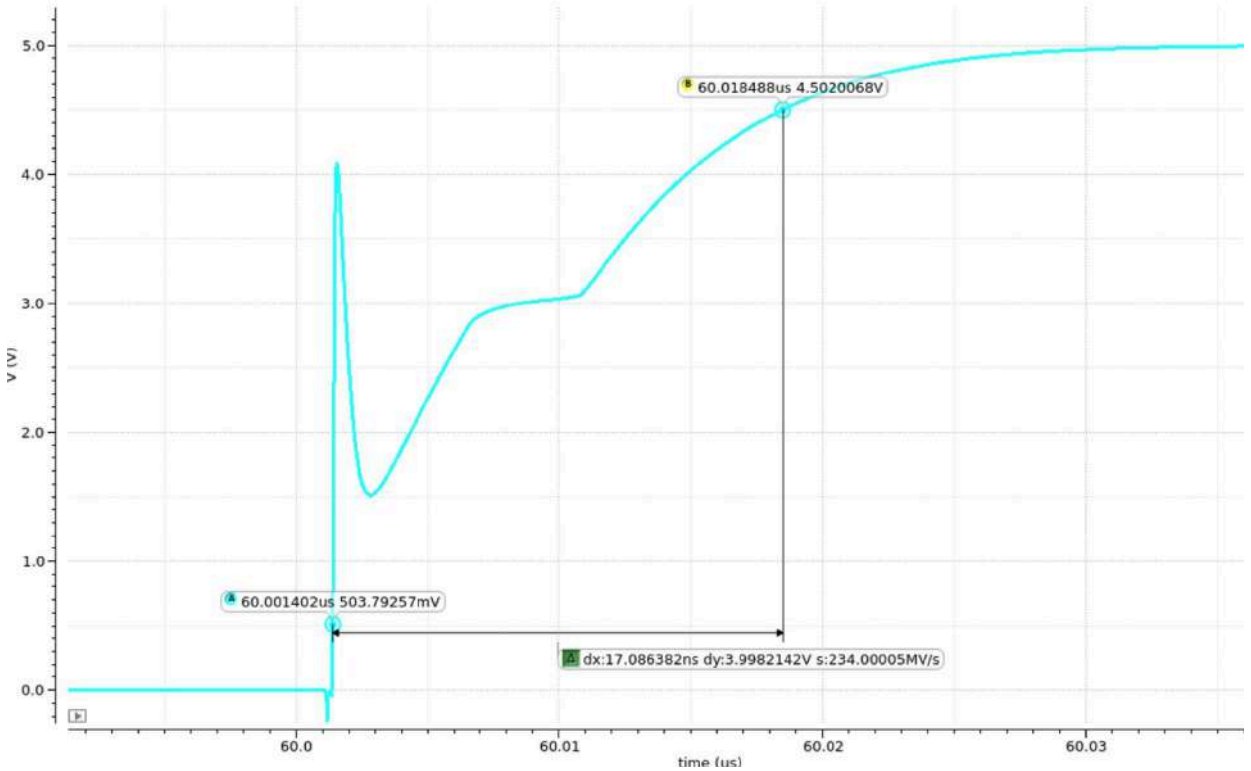


Figure 3.13 – Rising edge of Vgate

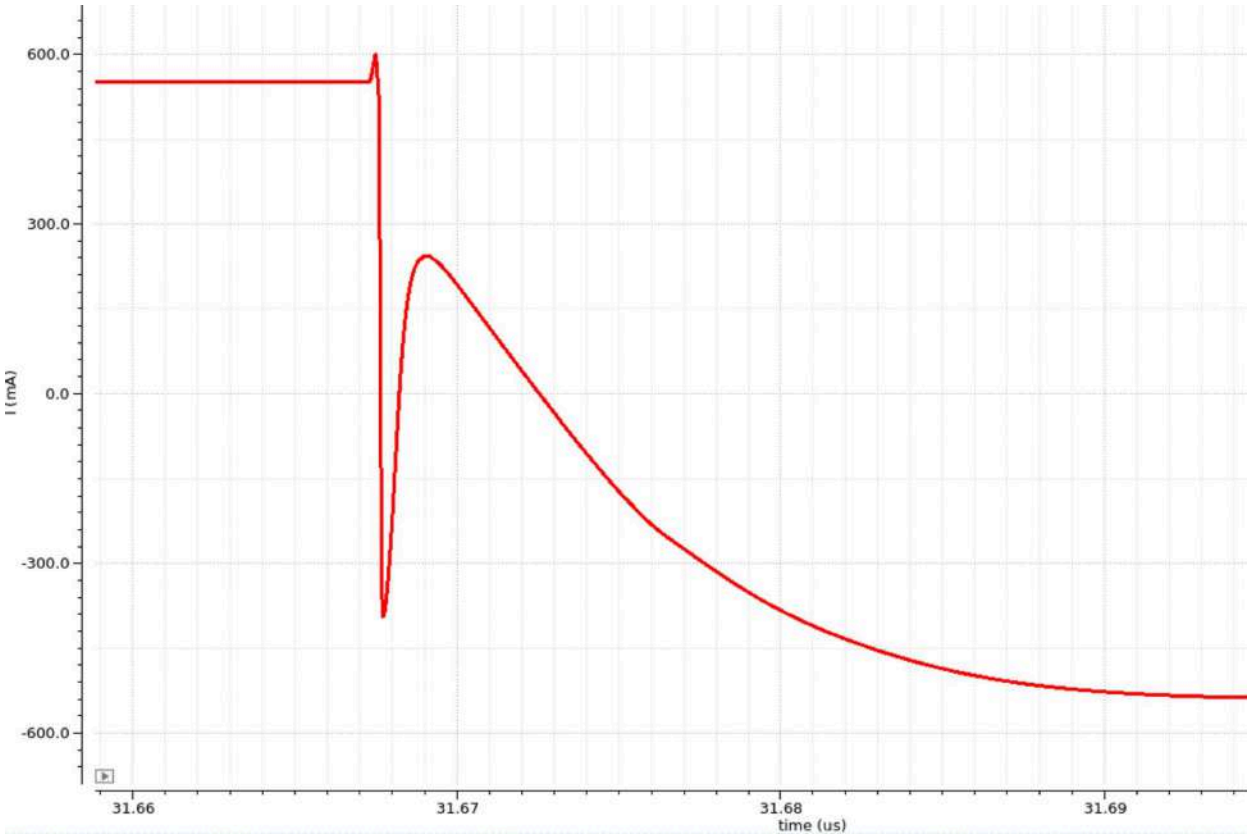


Figure 3.14 – Falling edge of Vgate

The Transient Response Analysis. The waveforms of Vgate show the predicted result for a fast and uncontrolled gate driver: fast rise/fall times (less than 20ns), unconstrained slew rate (dV/dt), minimal power losses and parasitic inductance in the loop. As a result, the switching event is immediately followed by voltage ringing and large overshoots. And the ringing itself signifies potential EMI issues.

EMI Analysis. In order to estimate the EMI potential for this and other topologies, a Discrete Fourier Transform (DFT) will be applied to the windowed time-domain signal on the power MOSFET drain voltage. After that, the magnitude will be converted to a logarithmic dB scale.

The frequency-domain representation $V(k)$ of the sampled drain voltage $v_{drain}[n]$ is defined as

$$V(k) = \sum_{n=0}^{N-1} \left(v_{drain}[n] \cdot w[n] \right) e^{-j\frac{2\pi}{N}kn} \tag{3.4}$$

where k is the frequency bin index ($0 \leq k \leq N-1$),

N is the total number of samples ($1,000,000$).

$v_{drain}[n]$ is the discrete sample of the drain voltage at time t_n.

$w[n]$ is the windowing function applied to minimize spectral leakage.

$$w[n] = 0.5 \left[1 - \cos\left(\frac{2\pi n}{N-1} \right) \right] \tag{3.5}$$

A Hanning window $w[n]$ is applied to the time-domain data to prevent spectral leakage caused by the finite observation interval (such as discontinuities at the start and end of the sample window).

The final spectral magnitude is expressed in decibels (dB) and calculated from the magnitude of the complex DFT result

$$V_{EMI}(f) = 20 \cdot \log_{10}\left(|V(k)| \right) \tag{3.6}$$

Additionally, such parameters will be used:

Observation Interval: $t \in [15\mu s, 100\mu s]$ (skipping the startup time of some circuits).

Sampling: the signal is discretized into $N = 10^6$ equidistant points.

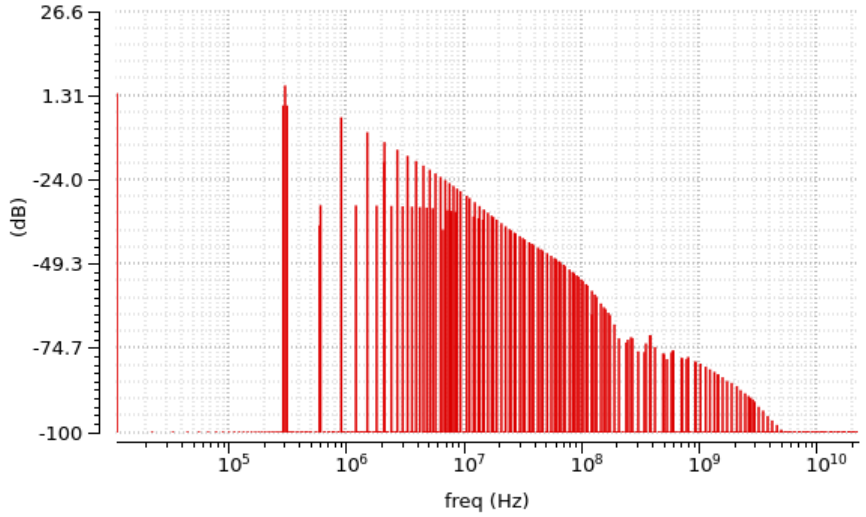


Figure 3.15 – EMI spectrum of push-pull gate driver

The resulting spectrum shows the traits of a "hard-switching" event such as high harmonics amplitude, slow roll off and resonant peaks. The energy content is high at odd harmonics. There is also a -20dB/decade decay that extends noise energy into the 30-300 Mhz range. The LC tank excited by the fast transition edge is visible in the high-frequency band.

All the simulation results confirm the fact that push-pull gate driver topology is quite successful at high speed switching but fails in the EMI aspects that are critical for modern applications. The drive strength is fixed and there are no internal mechanisms of limiting the spectral bandwidths of the fast switching edges and dampening the ringing. While this topology still finds its application, to meet the EMI standards it requires a bulky expensive filtering solution outside the circuit. Another important aspect is that this topology is at the mercy of the environment. If the temperature changes, the switching losses increase. If the Vdd voltage suddenly increases, the circuit may show even more emissions. Altogether, these limitations push to the necessity of exploiting other topologies, preferably with active control.

3.3 The Digitally-Controlled Segmented Driver (State-of-the-Art)

3.3.1 Architecture and Segmentation Strategy

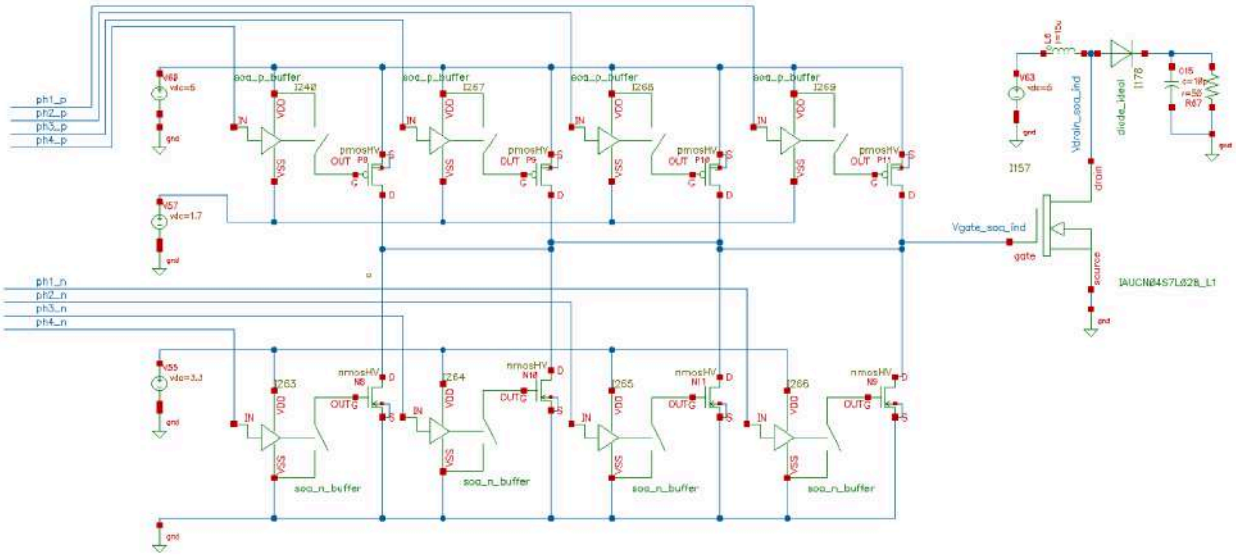


Figure 3.16 – The state-of-the-art testbench schematic

A digitally segmented gate driver is a logical advancement of the regular push-pull gate driver. While it still lacks the feedback control and is not fully analog, it shows the potential to improve some of the serious drawbacks of the regular gate driver. Structurally, this topology remains a push-pull gate driver that does the same action as before, charges and discharges the gate of the power MOSFET. The difference here lies in the number of buffers. Instead of using one tapered buffer for push and one for pull, each buffer is divided into four identical parts (called legs in this paper) that are connected in parallel. So instead of a chain of six inverters there are four chains for push and four chains for pull side. The core idea is that the drive strength is represented by the number of legs that are active at a specific moment [24]. The activation of the legs is made possible using a digitally controlled block (which for the purpose of this thesis is implemented as Verilog-A module) called pwm_4_splitter.

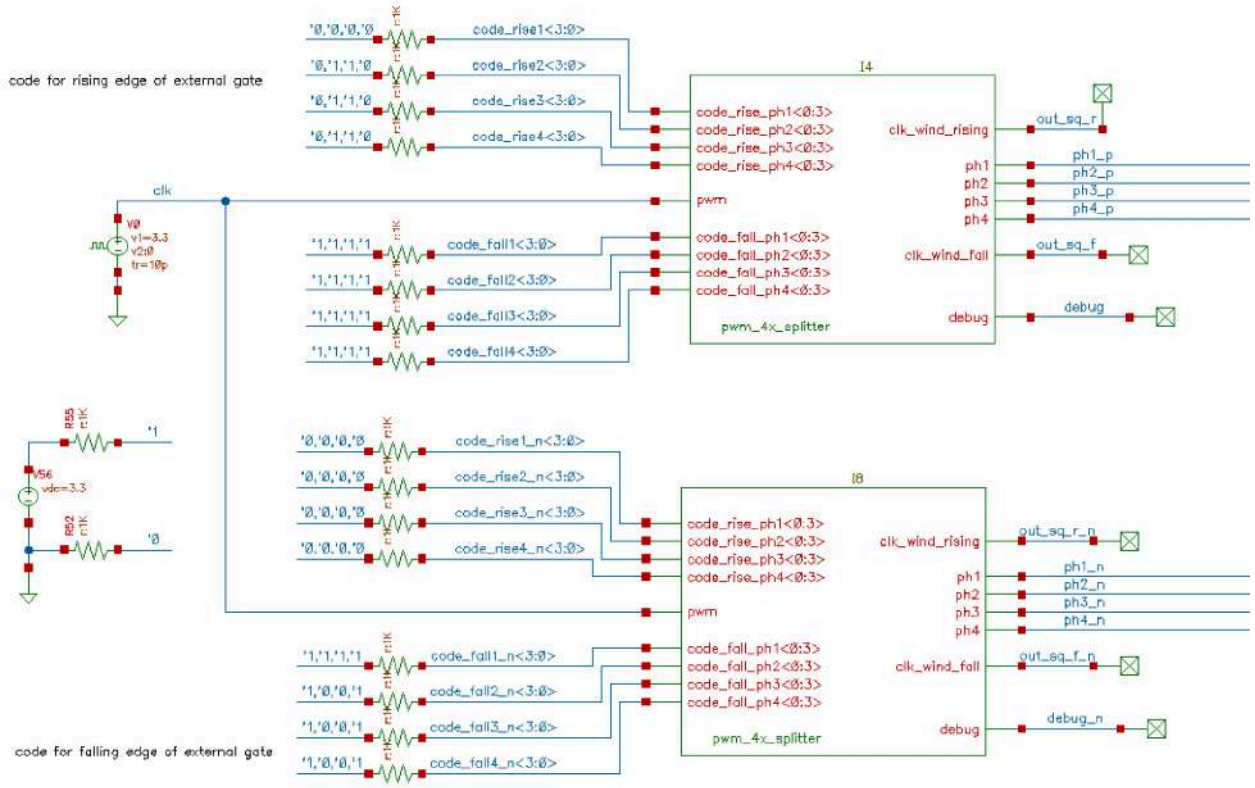


Figure 3.17 – Digital control block

On each rising and falling edge of the PWM signal, the block opens a finite modulation window. Time within a window is divided into four intervals: i = 0, 1, 2, 3. For each of four phases and for each of four legs, the 4-bit code pattern determines if the leg should be active. The rising and the falling edges have their own code patterns so there is opportunity to shape them independently.

When the block detects the rising edge of PWM it resets the internal counter and starts a 4-phase timing sequence. At each phase the block looks at bits in the 4-bit code pattern for each leg and drives the signals ph1 - ph4 that are connected to Vgate of each leg. The leg is enabled if the bit in the code pattern is ‘1’ and disabled if code is ‘0’. The same with the falling edge using a separate ‘falling time’ set of codes. The number of active legs and the effective output resistance are piecewise-constant functions of time during each transition.

Since the sizes of all legs are identical, the gate current that is driving a phase corresponds to the number of enabled legs. The driver behaves like a source with effective resistance as Rleg is the on resistance of one leg and N(i) is the number of legs active during the phase. This corresponds to the equation:

$$R_{eff}(i) = \frac{R_{leg}}{N(i)} \tag{3.7}$$

If the power MOSFET's gate is mostly capacitive with a nonlinearity around MIller plateau, the gate current during the phase can be presented as:

$$I_{gate}(i) \approx \frac{V_{DD} - V_{plateau}}{R_{eff}(i)} = N(i) \cdot \frac{V_{DD} - V_{plateau}}{R_{leg}} \tag{3.8}$$

The IGS current and its instantaneous gate capacitance determine how the Vgs slope looks. This means it is possible to shape the Igate and the timing of Vgs during on and off sequences by choosing the appropriate code words.

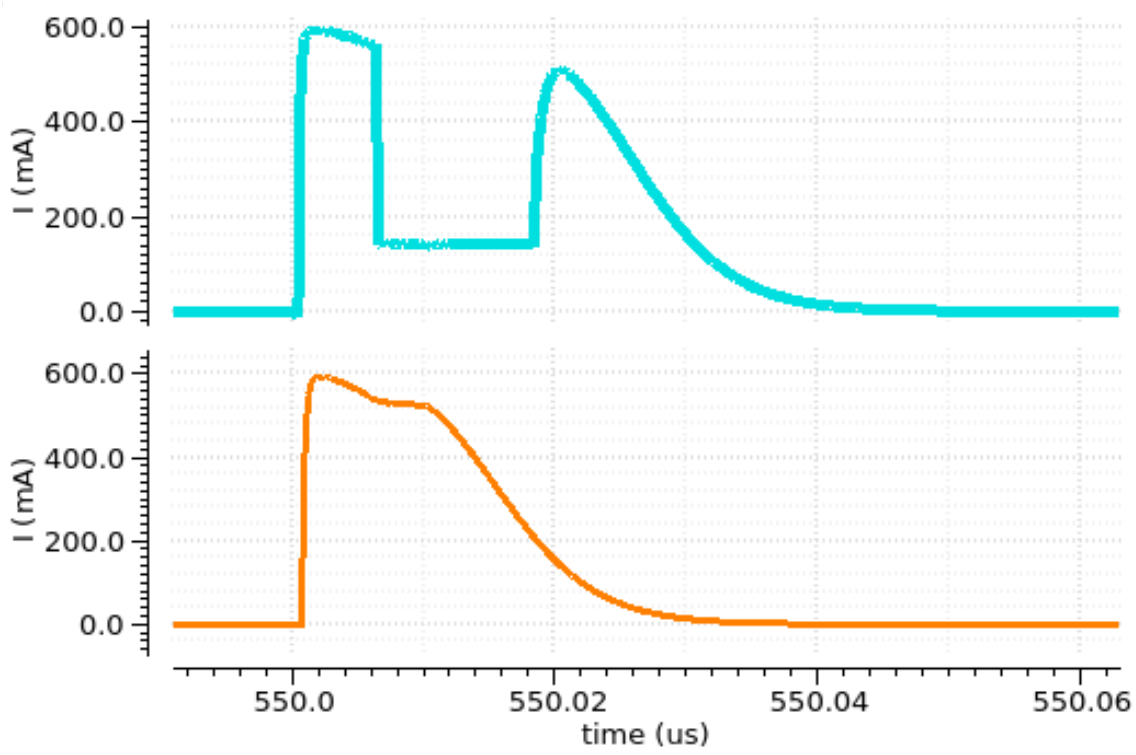


Figure 3.18 – Comparison of gate current of segmented gate driver (blue) versus push-pull (orange)

The pattern chosen for rising edge for this simulation may be illustrated like this:

Phase 0: [====] (Full Strength)

Phase 1: [=] (Weak)

Phase 2: [=] (Weak)

Phase 3: [====] (Full Strength)

The code for the first phases enables all legs. The two phases in the middle have only one leg enabled. The last phase has all four legs enabled. Physically, this sequence represents the fast rise of Vgs from 0. After that there is a gradual progression through the plateau. This is the place where the changes of Vds and EMI and switching losses are the most sensitive to the strength of gate drive. The final phase brings Vgs back to the final value by a strong gate drive. The similar pattern can be chosen for the falling edge. For example a strong drive at onset of turn-off to decrease time of a potential short-circuit interval and a weaker drive for decreased ringing at the end of conduction phase.

3.3.2 Practical Limitations and Design Challenges

An important aspect of this topology is the cost of the improvements compared to a simple push-pull topology. Splitting the output stage to multiple legs increases area, parasitic capacitance and design complexity. Each leg requires additional routing and asymmetry between legs will translate into unequal delays and different behavior during switching events. Process, voltage and temperature corners are more important than in the case of a fixed-strength push-pull driver.

A fundamental limitation is the nature of control as the driver strength can change in discrete steps at discrete times and the number of code possibilities is large. Despite choosing a specific pattern, the Vgs waveform still shows abrupt

enabling/disabling of entire legs. This inevitably produces disturbances in the time domain on the VGS voltage whenever the pattern changes. In the frequency domain it shows a more fragmented spectrum in which energy is not eliminated but rather redistributed. Such architecture cannot produce a continuously shaped or optimised Vgs [25].

The effectiveness of the segmented gate driver mostly depends on the stable operating conditions and the choice of codes. The codes are typically fixed or configured once per application. If the operating conditions like DC voltage, temperature or load change, the code pattern may not be efficient anymore. This topology remains an open loop solution, just offering better tradeoff than a simple push-pull gate driver. Without any sort of feedback this scheme may not seem reliable as it cannot compensate for variations in parasitic inductances, device parameters or external constraints like EMC limits.

3.3.3 Simulation Results and Baseline Characterization

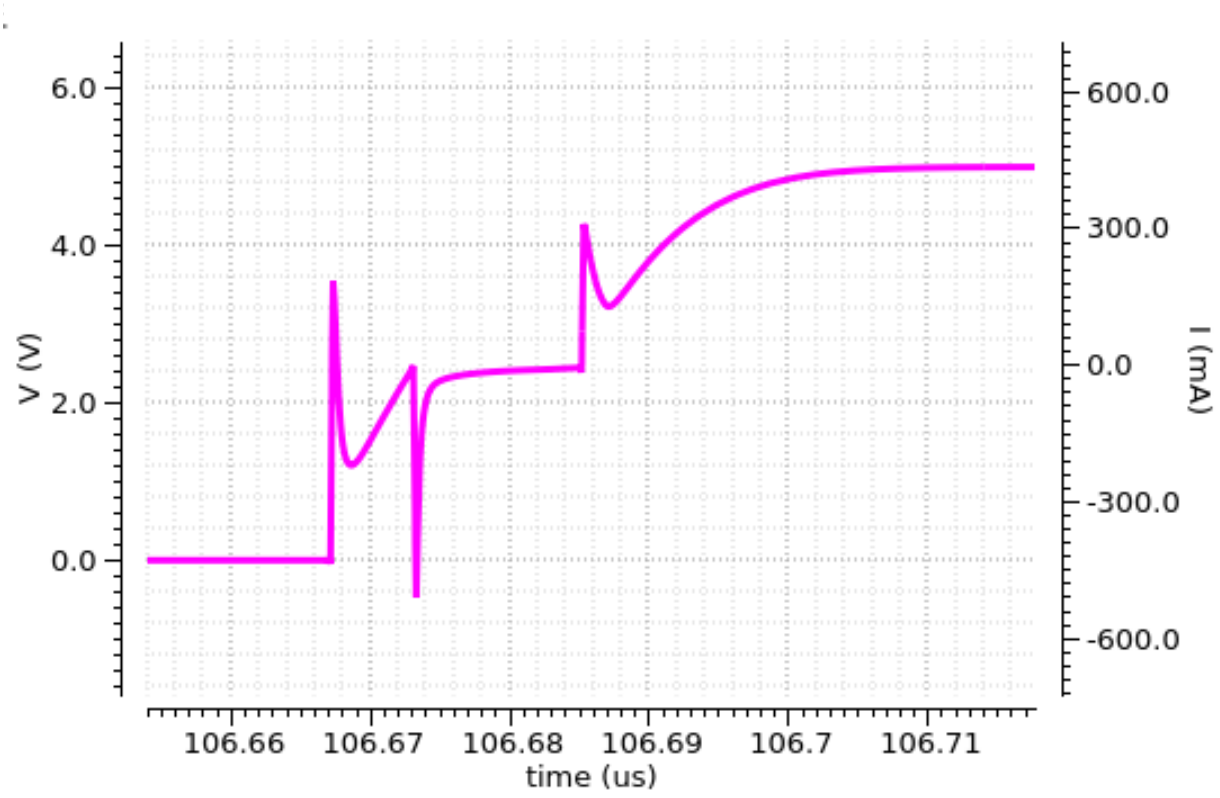


Figure 3.19 – Vgs of segmented gate driver.

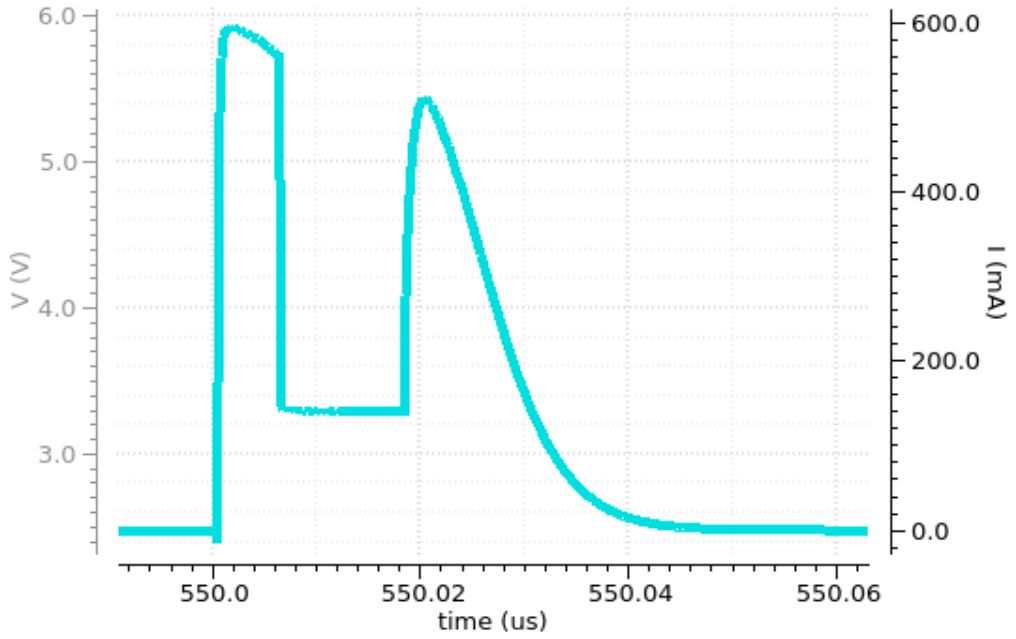


Figure 3.20 – Igate of segmented gate driver.

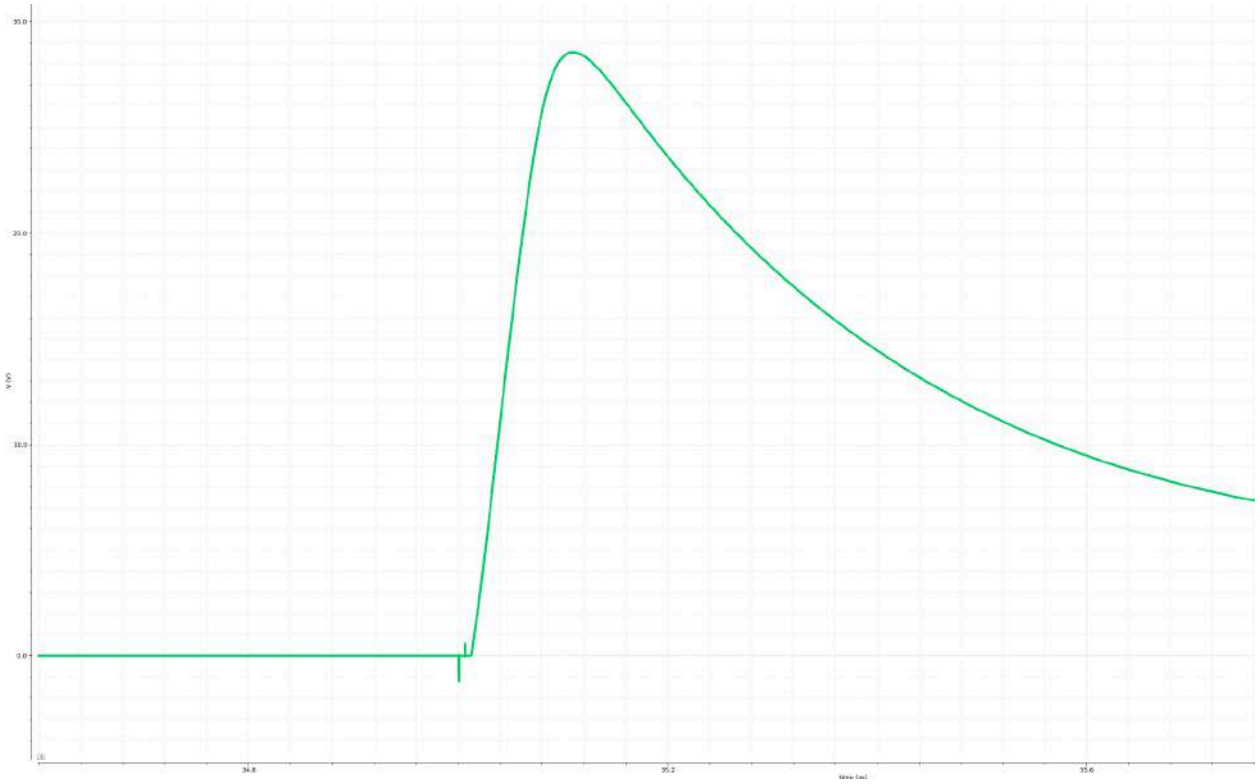


Figure 3.21 – The rising edge of Vds of the power MOSFET.



Figure 3.22 – The falling edge of Vds of the power MOSFET

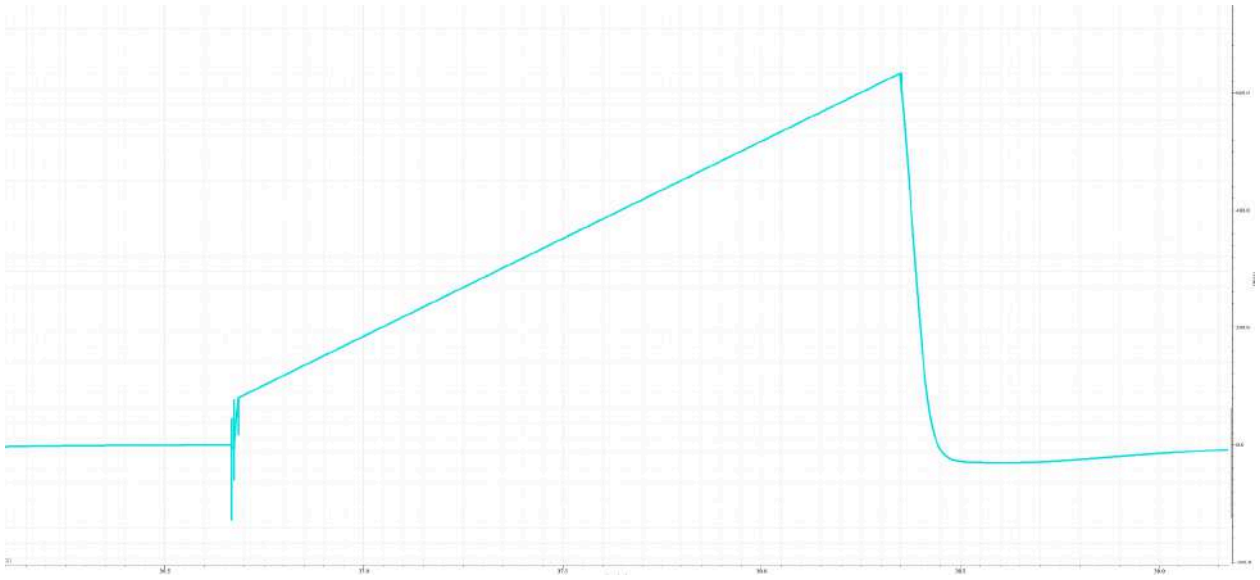


Figure 3.23 Ids of the power MOSFET

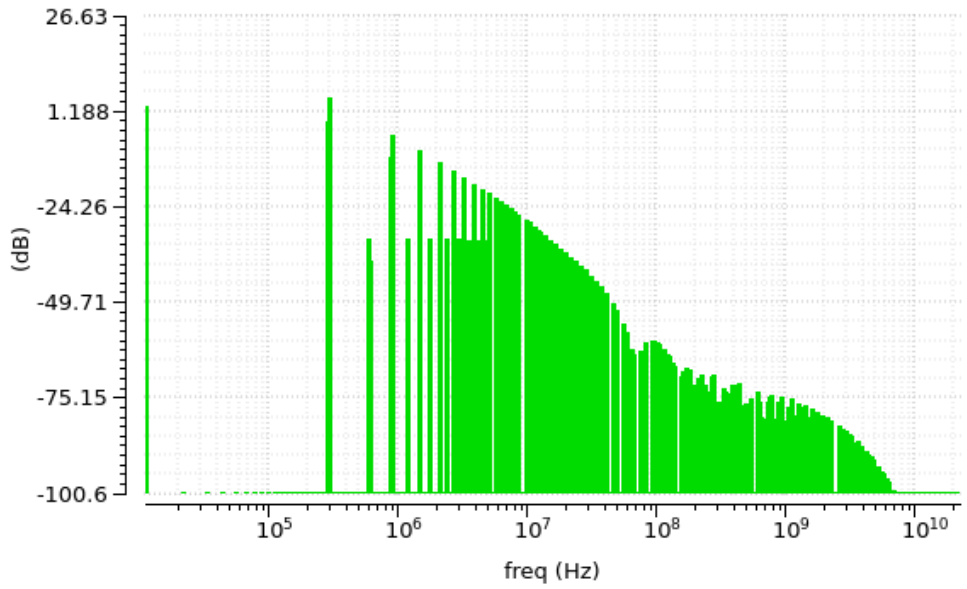


Figure 3.24 – EMI of segmented gate driver.

The waveforms show slightly different behavior compared to the simple push-pull gate driver. Vgs evolves as a continuous function with distinctive changes in the slopes of four phases. The gate current shows four discrete steps that represent the pattern of gate strength 4-1-1-4. As a result, the Vgs charge trajectory during the Miller plateau is stretched and reshaped in a controlled manner showing a less aggressive transition while still achieving the target switching time. The limitation of Igate at the moment when the power MOSFET's drain voltage is switching reduces peak dV/dt at switching node and dI/dt in the commutation loop. This helps to slightly lower the EMI though relatively large overshoots and underdamped ringing characteristics are still visible on the all waveforms including Vgs, Igs, Vds and Ids. Another significant advantage of the segmented drive circuit is the fact that changing the patterns does not require any changes in the schematic and layout. Using another pattern is all that's necessary to completely reshape the way the gate driver works. Any observed performance differences (in EMI or efficiency) rely solely on the active control strategy and not on the differences in peak current capability or total capacitance.

This circuit will serve as the baseline for our comparison with the OTA based gate driver presented in the next part of this chapter.

3.4 OTA-Based Gate Driver

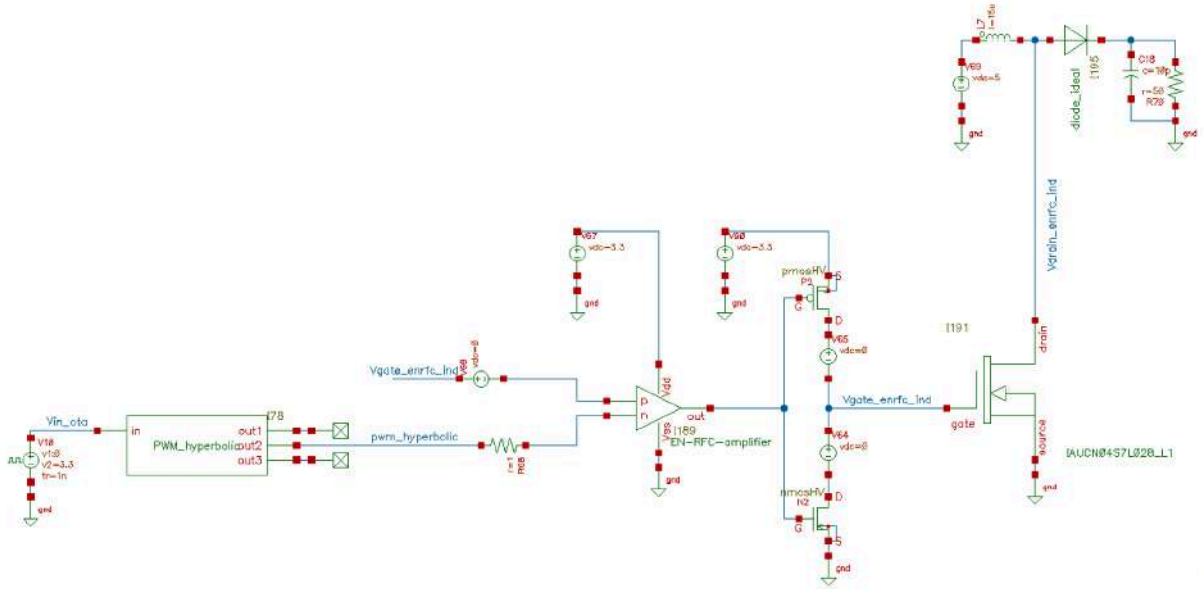


Figure 3.25 – OTA-Based Gate Driver

3.4.1 Overall concept of the OTA-based gate driver

The gate of power MOSFET in this architecture is no longer driven directly by a digital signal or a preprogrammed segmented driver. Instead, it is placed inside a feedback loop of an operational transconductance amplifier whose job is to force the Vgs to follow the reference waveform. At first, the digital PWM signal is passed through the high-order “hyperbolic” filter implemented in Verilog-A. The output of this block is a smooth curve with a specified 10-90 % transition time that serves as the reference input of the OTA. Then, the actual gate voltage of the power MOSFET is sensed and fed back to the negative input of the OTA which continuously computes the error between the desired and measured Vgs and converts this error into control current. Since OTA cannot deliver the large currents required to charge and discharge the MOSFET gate itself, its output drives a push-pull buffer stage of the same size as the previous topologies.

As discussed in chapter 2, the drain-source voltage waveform and the associated EMI are strongly influenced by the way in which the gate charge is

passed through the Miller plateau. The OTA's closed-loop control of Vgs provides a powerful way of shaping the switching transients. The reduction in overshoots and spectral content depends directly on the capabilities of the chosen OTA topology, which leads to the comparison between the available options.

3.4.2 The choice of OTA topology

The choice of OTA topology for the job is the most important part as it determines how accurately and how fast the feedback loop can force the Vgs of power MOSFET to follow the reference curve. All reviewed topologies operate in the same configuration as shown before using the same load and having to manage the same parasitics. When the reference curve begins a transition, the OTA must slew the gate node along the curve, sourcing or sinking enough current to follow the curve without large error or delay. Any limitation in DC gain, bandwidth or slew rate directly results in the inability to precisely follow the reference. The basic cascoded OTA with an output stage and a simple compensation network is assumed to fail with at least one of the requirements so it will be compared only occasionally.

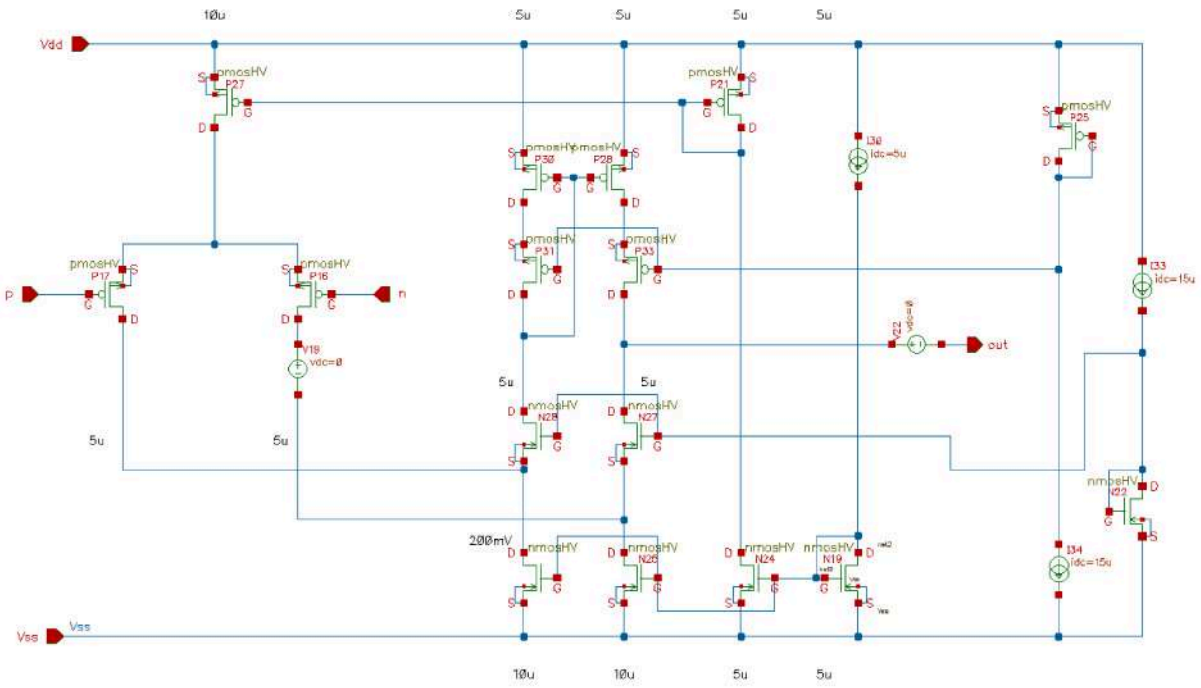


Figure 3.26 – Folded-cascode OTA

While the classical folded-cascode OTA provides high intrinsic gain and sufficient bandwidth for small-signal tracking, its large-signal transient performance is limited [30]. The maximum current available to charge the internal compensation nodes and the output buffer is limited by the fixed bias tail current. When the driver needs to make a fast transition, the OTA immediately saturates, entering a slew-rate-limited regime where the feedback loop effectively breaks [31]. In the context of this research, this architecture does not suit the needs. The simulation results show that it takes almost 400ns for the OTA to transition while the goal is to fit into 40ns. The gate voltage curve is determined not only by the shape of the reference but also by the OTA's internal saturation limits. Additionally, the gate voltage cannot reach the expected voltage level of 3.3V within the given time and starts falling.

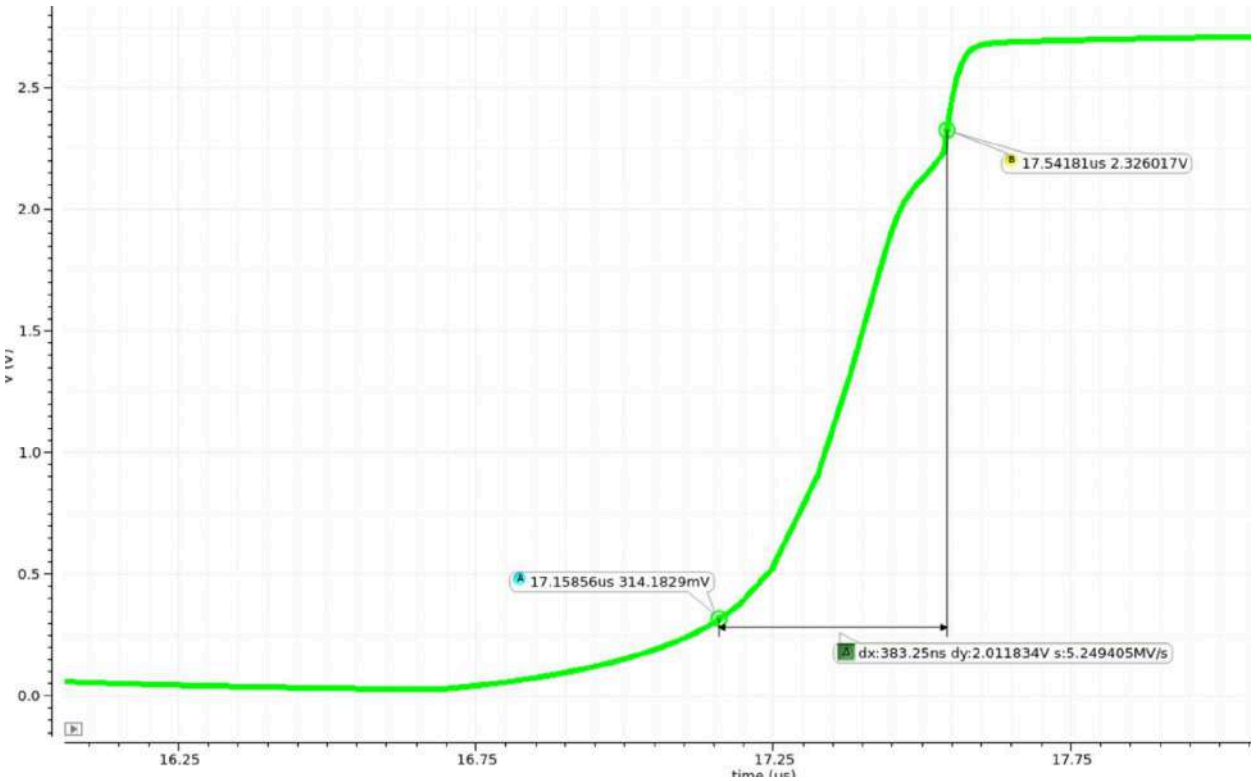


Figure 3.27 – Vgs of folded cascode

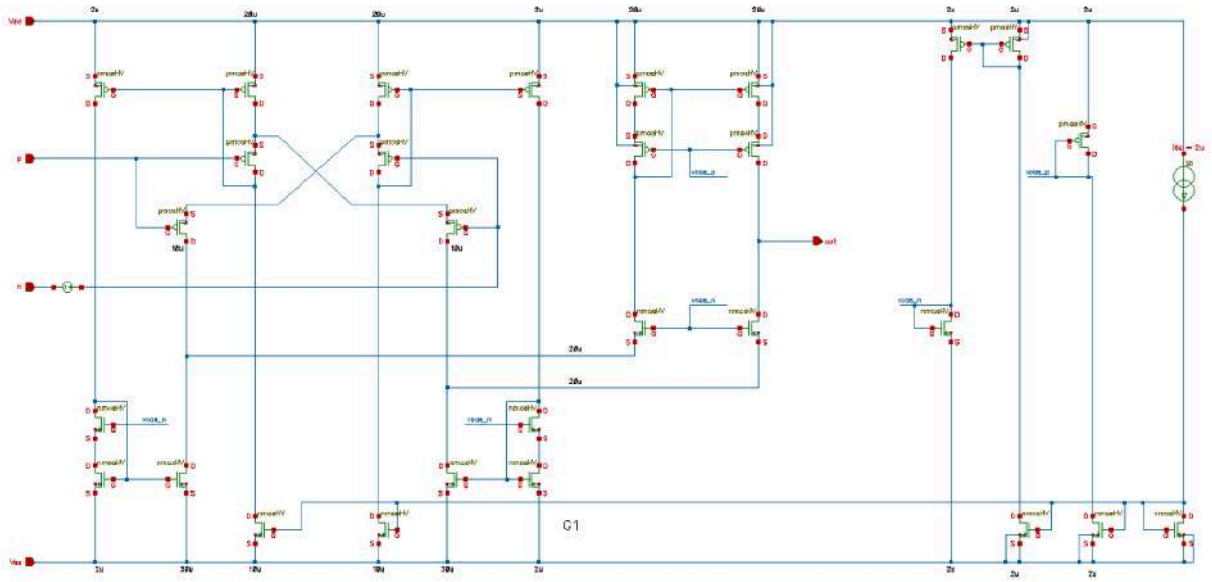


Figure 3.28 – External nonlinear current recycling folded cascode OTA

The nonlinear current-recycling folded cascode amplifier described in this work [26] is a highly attractive candidate for the purpose of being a core of a gate driver. This amplifier remains a folded cascode as the input differential pair is “folded” into a high-impedance gain node, allowing large output swing while maintaining high intrinsic gain. The improvement over a regular folded cascode lies in the addition of a flipped-voltage follower-based adaptive biasing scheme [27] and nonlinear current-recycling branches [28]. Two nonlinear current mirrors are used to recycle and redirect boosting currents from the input stage back into the signal path when large transients occur. As a result, the small-signal gain and gain-bandwidth product remain comparable to a conventional folded cascode under quiescent conditions, while the effective transconductance and available output current increase dramatically when the differential input error becomes large. The article reports 2.4-fold gain-bandwidth and 14-fold slew-rate enhancements relative to a regular folded cascode at unchanged static power consumption [26].

The OTA’s job is not only providing high DC gain to minimize the steady-state error between the reference curve and the actual Vgs, but also responding fast when the reference initiates a transition and the instantaneous tracking error between inputs is large. At the beginning of such transition, the

amplifier is required to source or sink current into the gate-driver buffer in order to move large amounts of current through the Miller plateau. Once internal nodes in a conventional folded cascode with fixed bias currents saturate, the output slope is bounded by the tail currents, and the loop temporarily loses the ability to follow the desired Vgs curve[29].

$$SR \approx \frac{Itail}{C_L} \tag{3.9}$$

By contrast, the nonlinear current-recycling folded cascode can draw additional current through its recycled paths and flipped-voltage-follower biasing, therefore during the initial part of the rising/falling edge the effective transconductance and output drive are significantly higher than in purely small-signal operation. The gate voltage can be brought close to the reference curve much faster, while preserving the high internal gain of the amplifier[27]. Once the large-signal error has been reduced and Vgs approaches the reference, the adaptive biasing in the current-recycling architecture gradually returns the OTA towards a lower-current operating point.

$$SR \approx \frac{Imax}{C_L} \tag{3.10}$$

where

$$I_{max} \approx \ kI_{tail} + I_{boost}(\Delta V), \qquad k > 1 \text{ ,} \tag{3.11}$$

$$I_{boost}(\Delta V) \propto (\Delta V)^2 \tag{3.12}$$

is the extra dynamic current created by the recycling/FVF action during large steps and k is the current mirror ratio factor. The slew rate can be approximated to:

$$SR_{enrfc} \approx \frac{k\, I_{tail} + I_{boost}(\Delta V)}{C_L} \tag{3.13}$$

In terms of gate-driver behavior, the amplifier differentiates between a slewing and a tracking phase within each switching edge. During the slewing phase it behaves as a strong, wide-bandwidth driver, capable of forcing the gate node to follow the desired curve despite the gate charge and Miller capacitance. During the tracking phase it reverts to a high-gain, lower-current folded cascode mode that maintains accurate following of the reference without excessive power dissipation. This kind of dynamic adaptation is difficult to make with a classical folded cascode, which is usually biased either for high slew rate with correspondingly high quiescent current or for low power at the expense of transient performance.

Such an architecture is expected to have two advantages over a regular folded cascode. First, the effective GBW product in the operating region may be much higher, which may allow the loop to follow the reference curve with smaller phase lag and amplitude error. This may lead to Vgs waveform that better reproduces the curve and thus to tighter control of dVgs/dt and the implied dVds/dt. Second, the improved slew rate ensures that the amplifier remains in a quasi-linear regime over a larger fraction of each transition. Instead of spending much of the rising/falling edge in a saturated, current-limited state where it behaves effectively as an open-loop driver, it retains sufficient loop gain to correct deviations from the reference, suppress overshoot and disturbances from parasitics. Moreover, the current-recycling concept is compatible with the presence of an external push-pull buffer as the additional current generated by the nonlinear mirrors primarily modulates the gates of the buffer transistors, which deliver the required gate charge to the power device. The nonlinear folded cascode serves as an adaptive control front-end for the buffer, which defines how aggressively the buffer should act based on the instantaneous tracking error, while keeping its own internal nodes near their optimal operating region.

3.4.3 Closed-loop unity-gain stability analysis vs input common-mode.

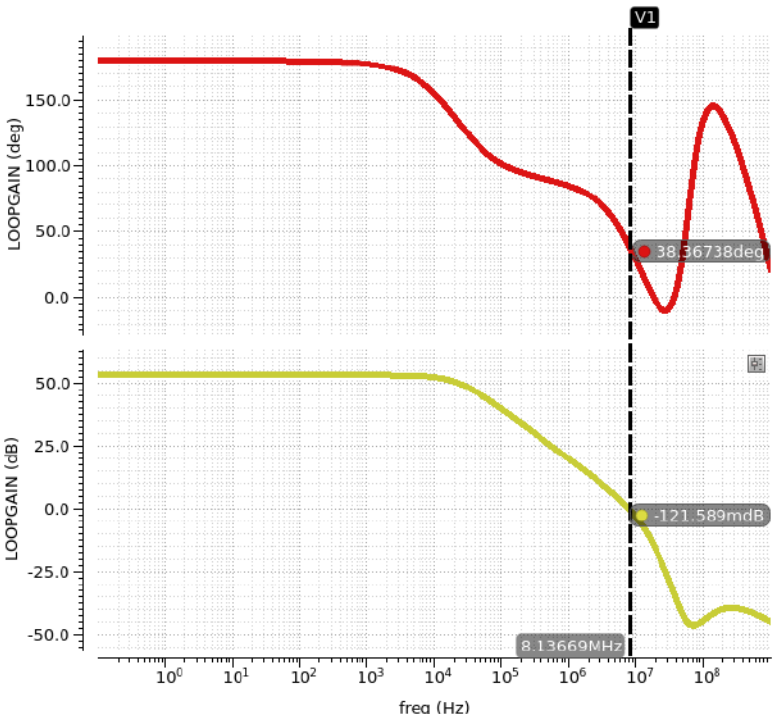


Figure 3.29 – ENRFC closed-loop stability analysis for DC common-mode level 0.5V

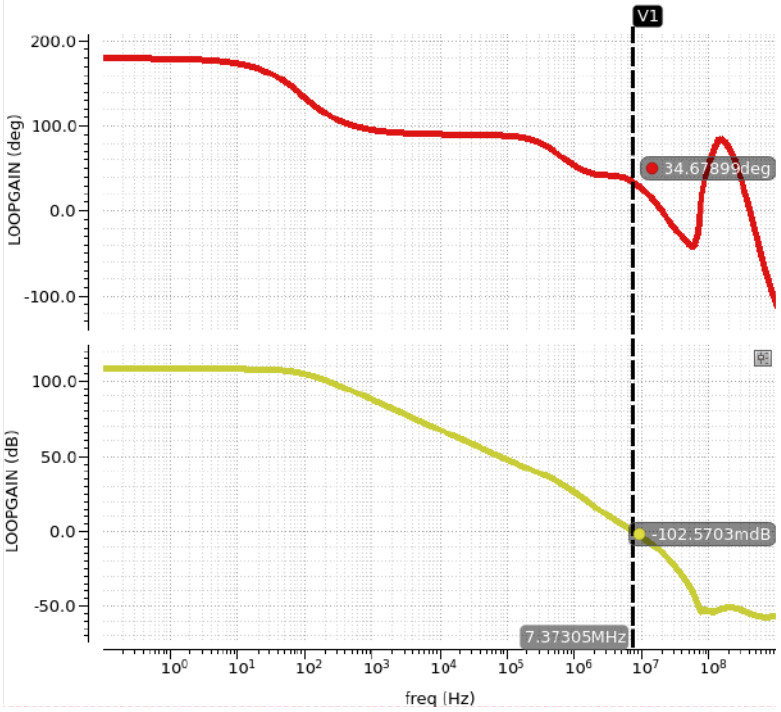


Figure 3.30 – ENRFC closed-loop stability analysis for DC common-mode level 2V

The OTA closed-loop stability was evaluated using STB (loop-gain) analysis. The voltage probe was inserted at the break between the feedback node and the inverting input. The non-inverting input was biased with a DC common-mode level Vcm. In a unity-feedback configuration driving the power MOSFET and the inductive load, the extracted phase margin is around 38 degrees at Vcm = 0.5V and around 35 degrees at Vcm = 2.0V, indicating marginal stability with limited robustness to operating-point shifts (bias/headroom changes move internal poles/zeros and reduce phase margin as Vcm increases). Further simulations are required to make a conclusion about the definitive stability of this topology for a given application.

3.4.4 Shaping the reference curve with the hyperbolic PWM filter

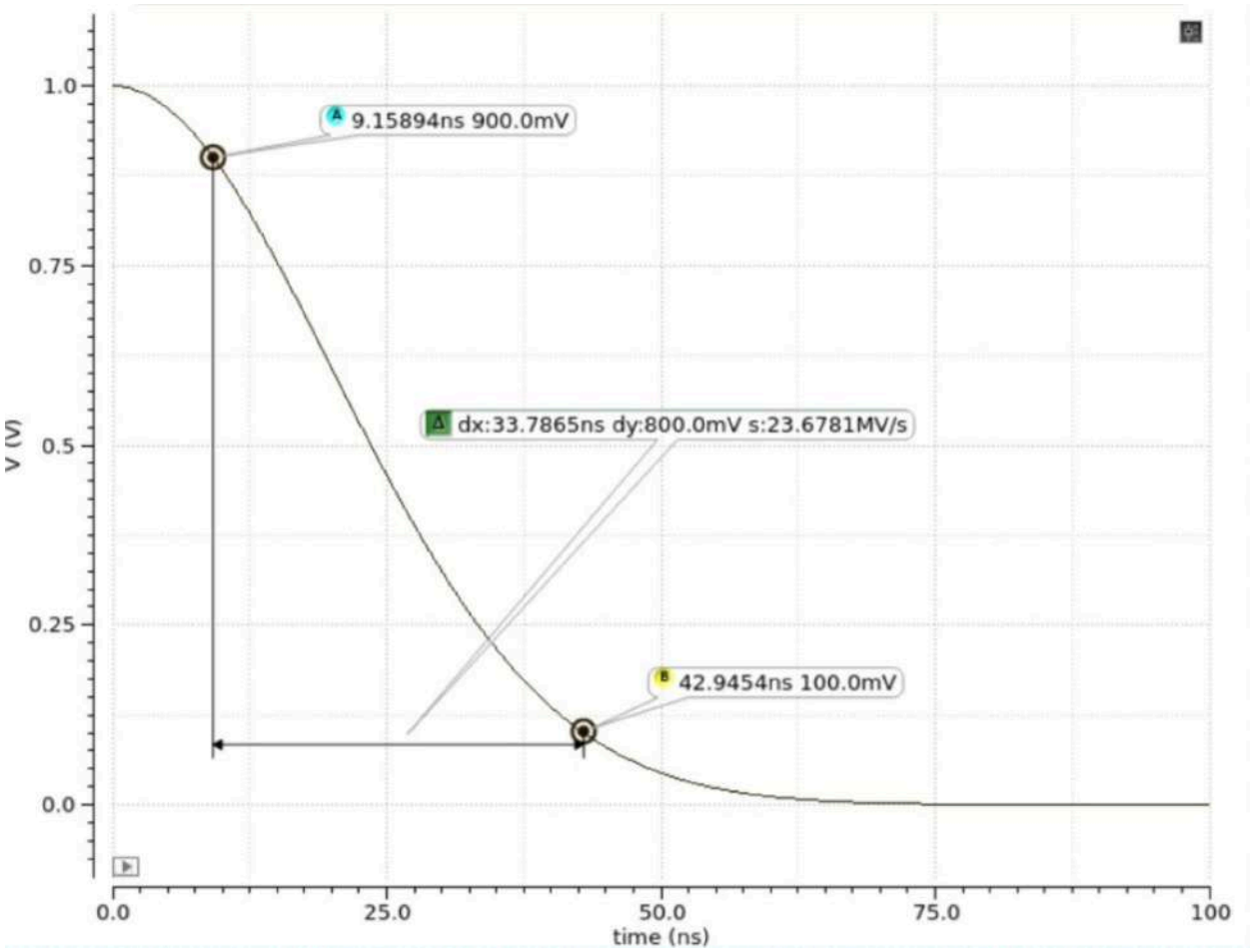


Figure 3.31 – The target curve to be turned into a filter

The first step toward shaping the Vgs of power MOSFET was to decide what kind of edge shape the driver should aim for. A target time-domain waveform was designed first - a smooth, monotonic decay from 1 V to 0 V with a characteristic duration of about 40 ns, a target switching speed of the gate driver.

At t = 0 the signal is at 1 V, and over the next tens of nanoseconds it falls in a way that is visibly more gentle than the exponential. The initial slope is relatively small with a broad mid-region with quasi-constant curvature and then the tail decays slowly towards zero. This shape in the time domain resembles one half of a symmetric impulse response and the other half would be its mirror image with respect to the vertical axis. If such a kernel is convolved with an ideal digital step, the result would be an edge that has no discontinuities and no abrupt breaks in slope. These are exactly the properties required for drain voltage in order to reduce emissions.

To be usable inside an analog circuit simulator, this kernel must be represented as a continuous-time, linear time-invariant (LTI) system rather than a discrete table of samples. An LTI system is characterised by its transfer function H(s), or equivalently by its poles and zeros in the complex s-plane.

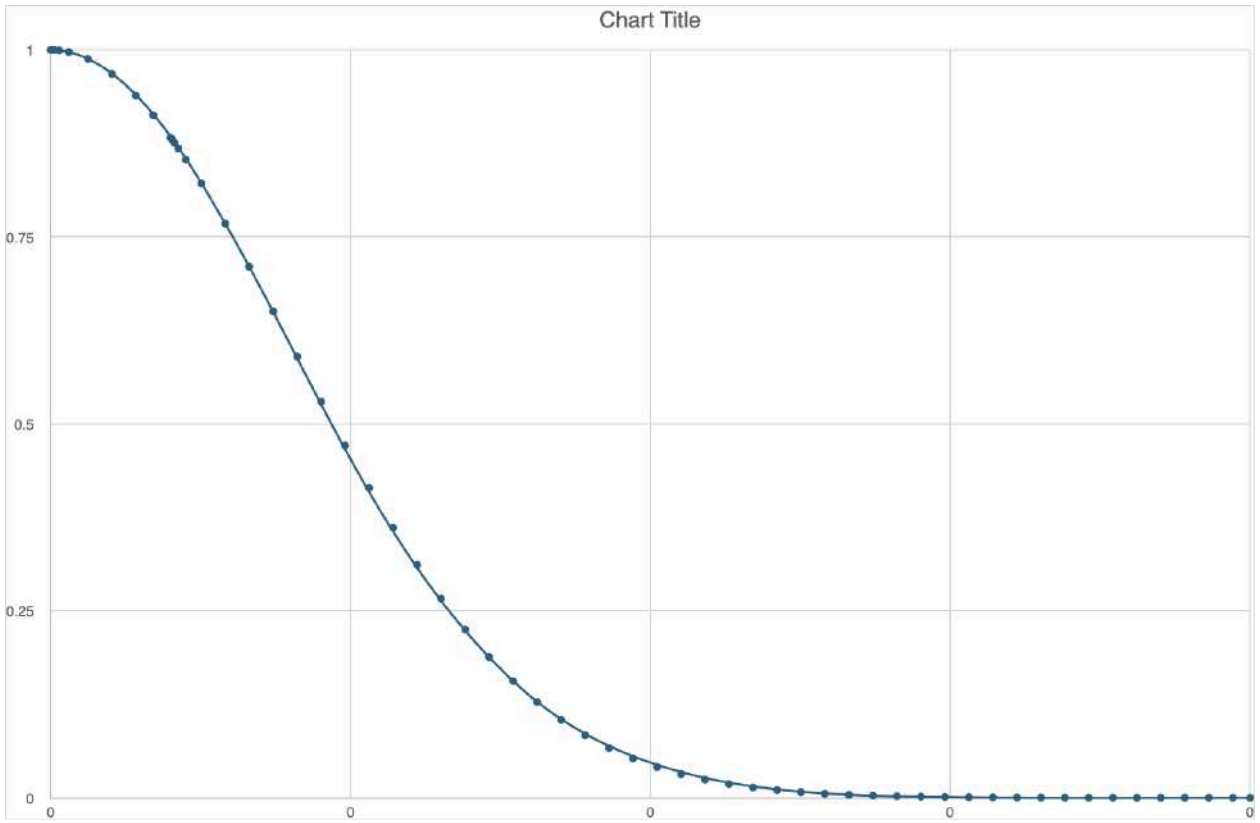


Figure 3.32 – The waveform generated from the tables

The waveform from tables generated from the simulation was interpreted as the step response (or equivalently, the time integral of the impulse response) of an unknown filter. A rational approximation problem was set up using MATLAB. The goal was to find a stable transfer function H(s) with only left-half-plane poles so that the simulated step response matches the sampled data. The outcome is a high-order filter whose impulse response reproduces the smooth decay seen in the original curve.

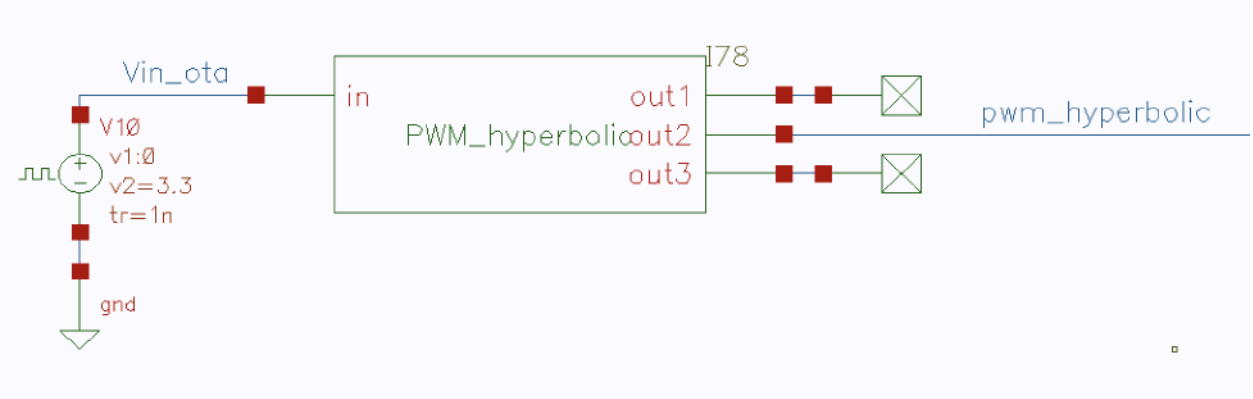


Figure 3.33 – PWM_hyperbolic Verolog-A block schematic

The pole-zero representation of this transfer function is what appears in the Verilog-A block PWM_hyperbolic. The arrays inside the code contain the real and imaginary parts of eleven complex-conjugate zero pairs and twelve real poles. All poles have negative real parts necessary for stability, and the conjugate symmetry of the zeros ensures that the resulting impulse response is real-valued. The high order of the filter is the price paid for reproducing the specific target shape. Only an LTI system with several separated time constants can approximate such behaviour accurately. Additionally, there is a scaling factor so multiplying all pole and zero frequencies by the same factor compresses or stretches the time axis of the impulse response. The same pole-zero pattern can be reused for any desired duration moving all poles and zeros to higher or lower frequencies producing the same transition. Such settings make the filter tunable without having to re-run MATLAB for every new rising time target.

```
V(out2) <+ laplace_zp(V(in), z, p, gain)
```

Figure 3.34 – Verilog-A implementation of the Laplace transfer function

This snippet is the resulting statement that realises this filter in the time domain. When the digital PWM input V(in) makes a step, the output V(out2) follows the continuous, hyperbolic-like trajectory defined by the transfer function. This resulting waveform is used as the reference curve for the OTA-based gate driver. The OTA observes the gate voltage through feedback and continuously

adjusts the gate drive so that the actual switching node follows the same hyperbolic curve as closely as possible.

3.4.5 Results, loop behaviour and qualitative comparison to segmented drivers

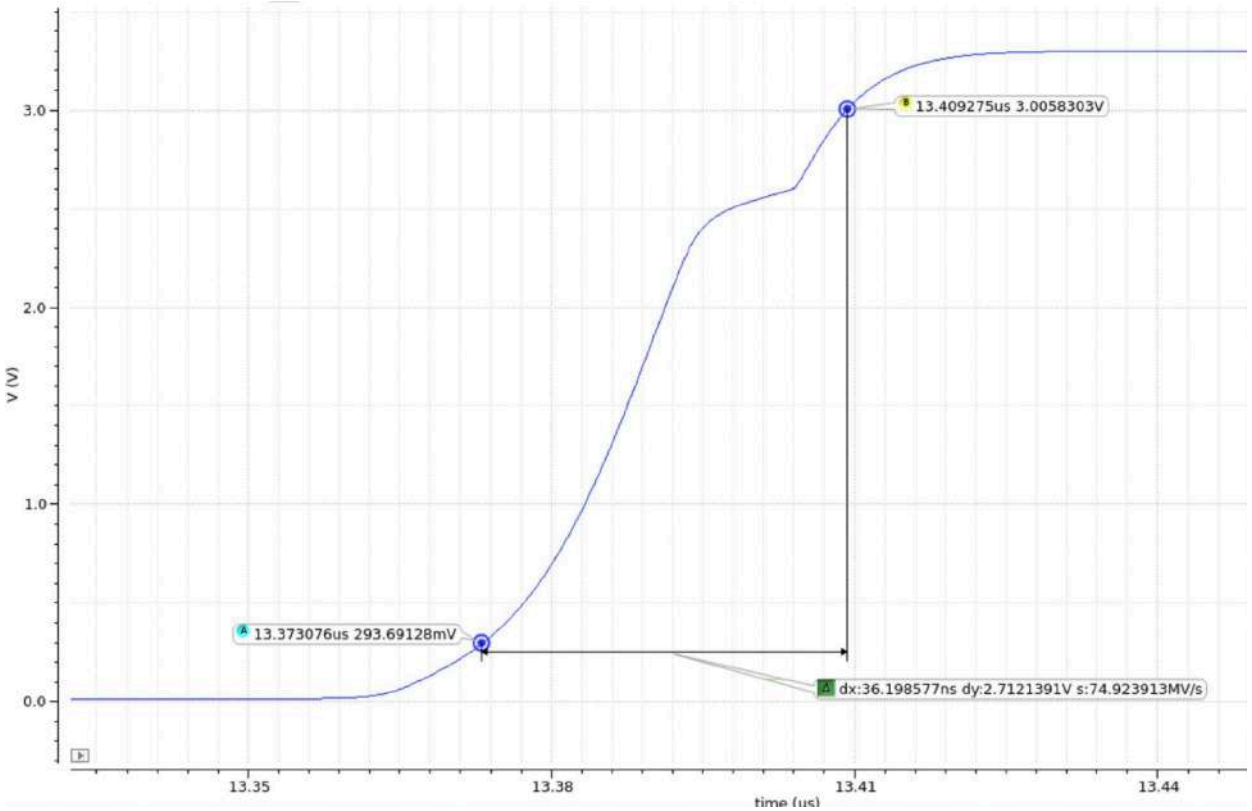


Figure 3.35 – The rising edge of Vgs of the OTA-based gate driver

The simulated waveform confirms the expected behavior. The Vgs plot of the OTA-based driver produces transitions that closely follow the reference curve. Vgs rises and falls as a smooth monotonic curve without the overshoot and underdamped ringing visible for both the conventional push-pull and the segmented digital driver. The deviation from the reference, except for a delay, is a small stretch with a visible Miller plateau.

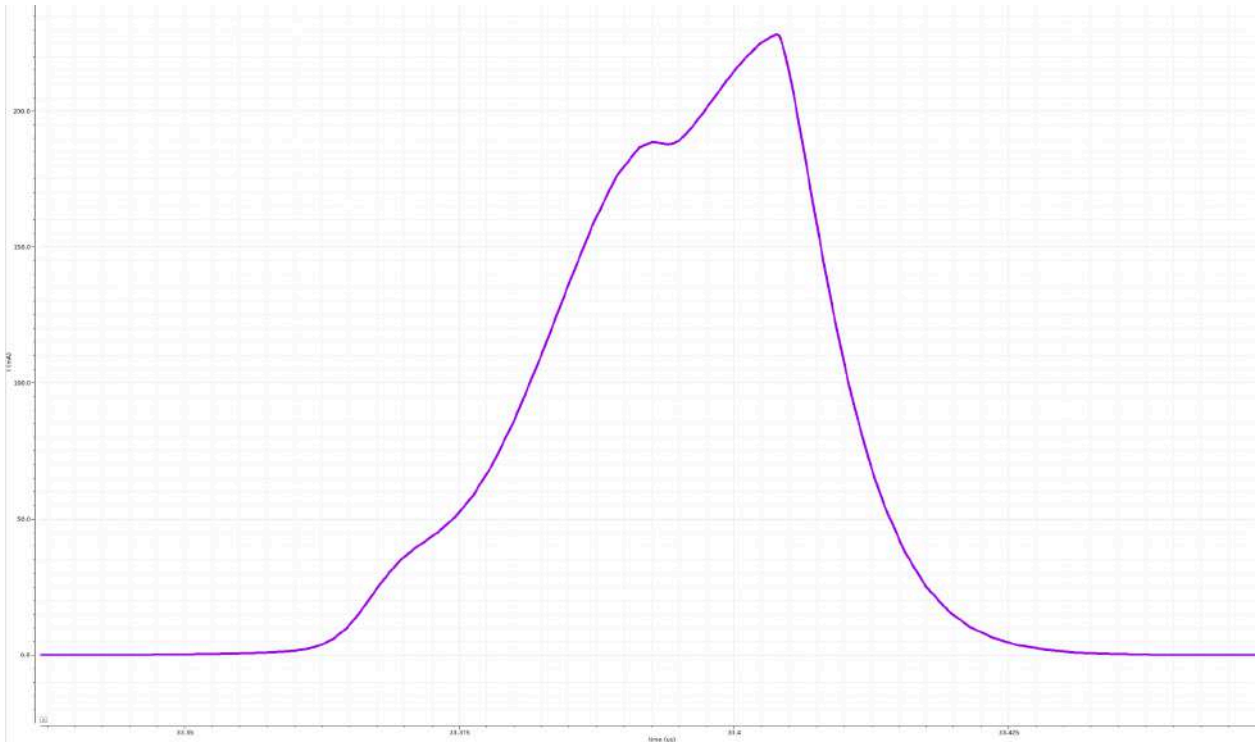


Figure 3.36 – The rising edge of Igs of the OTA gate driver

The Igs plot shows that the loop naturally shapes the gate current into a broad, relatively low-amplitude pulse rather than the narrow, high-amplitude spike like the open-loop drivers. Instead of charging and discharging the gate with short bursts of large current, the OTA supplies a moderate current over an extended interval. This limits dQg/dt and therefore dVds/dt during the most critical part of the transition.

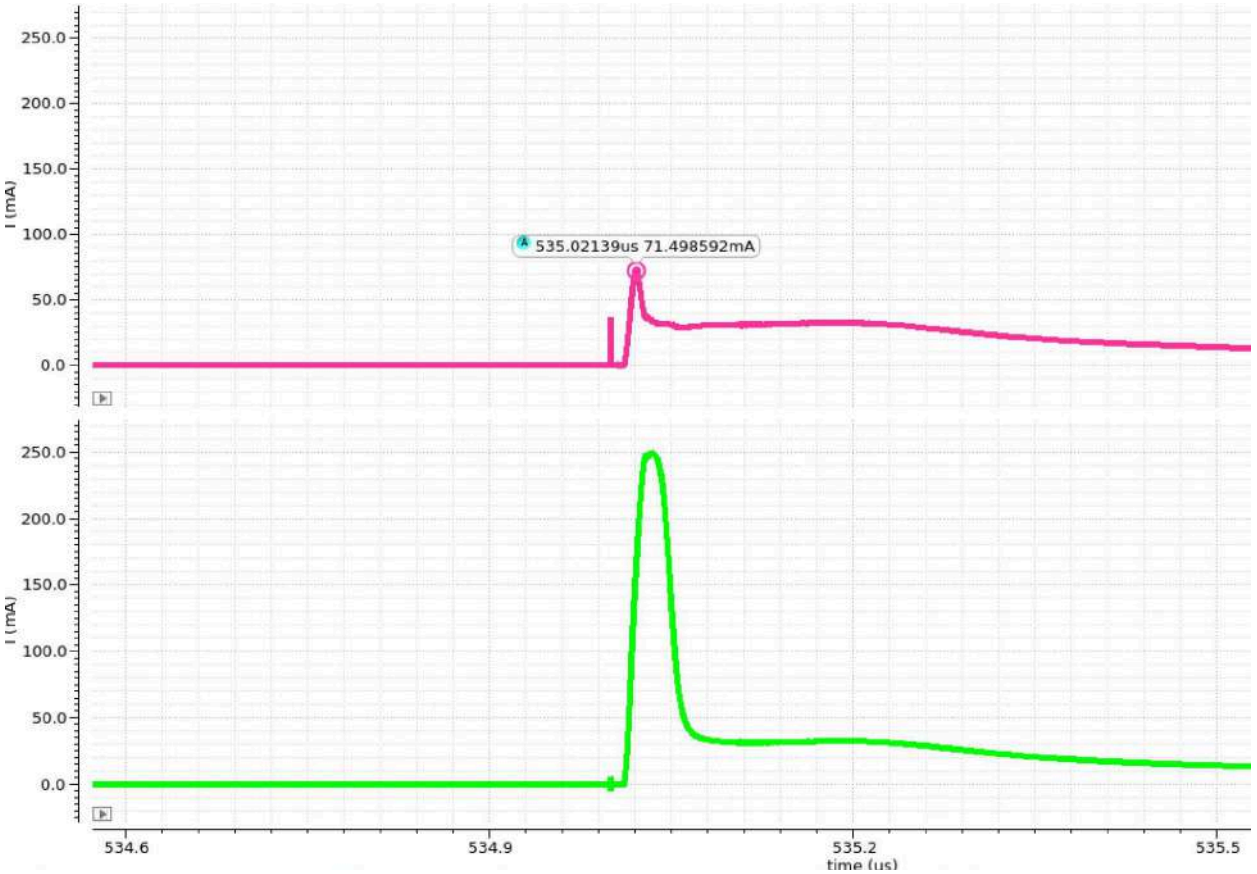


Figure 3.37 – High/low side currents of output stage during switching event.

The push-pull output stage of the OTA-based gate driver shows a cross-conduction of 70mA during a switching event.

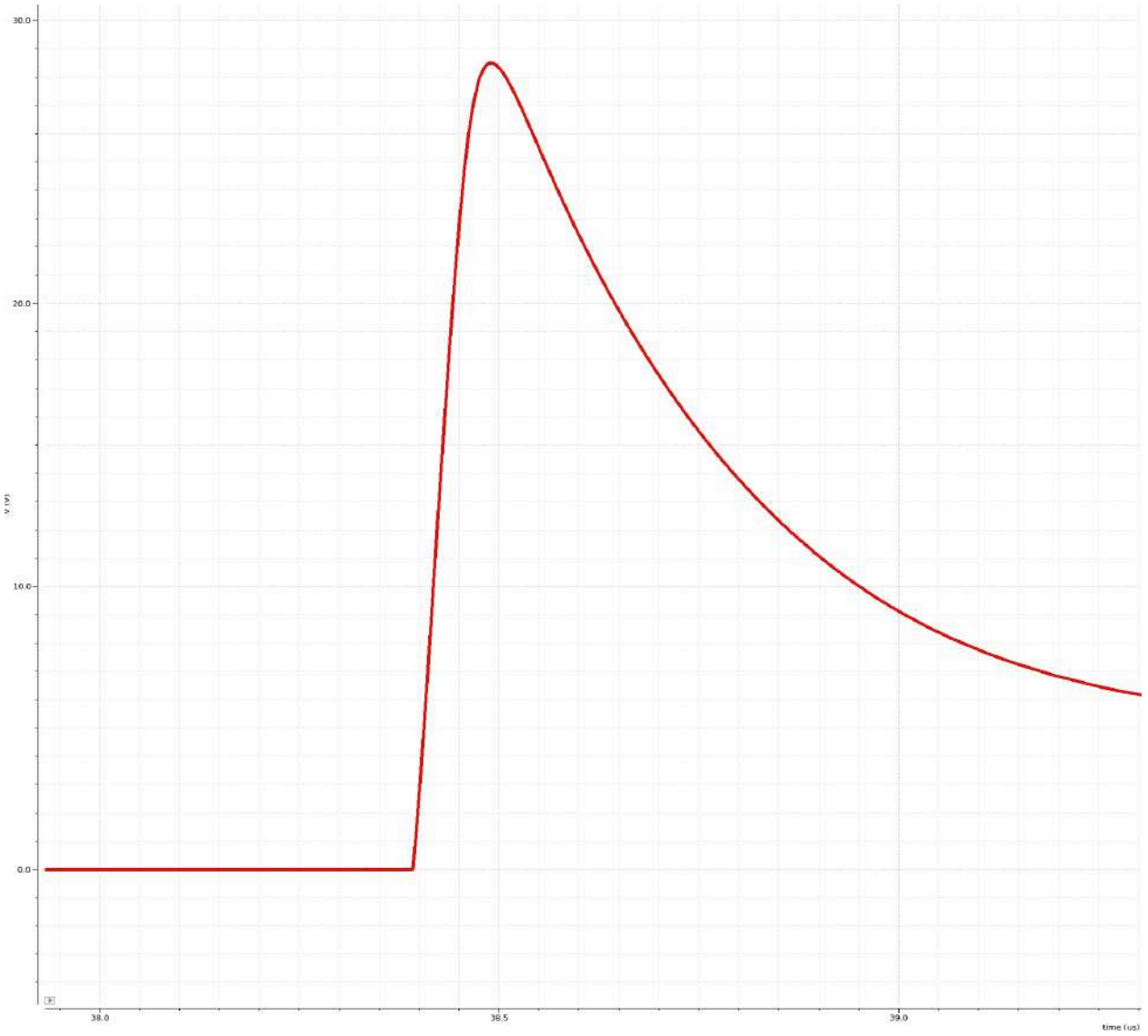


Figure 3.38 – The rising edge of Vds of the power MOSFET



Figure 3.39 – The falling edge of Vds of the power MOSFET



Figure 3.40 – Ids of the power MOSFET

The Vds transition does not exhibit sharp edges. The voltage rises and falls along a gently curved trajectory and settles to its final value with only a single, rapidly damped residual ripple. The drain current Id shows a smooth transition. The conventional and segmented gate drivers produce a much steeper change in Vds and distinct ringing in both Vds and Ids once the parasitic inductances in the commutation loop are excited.

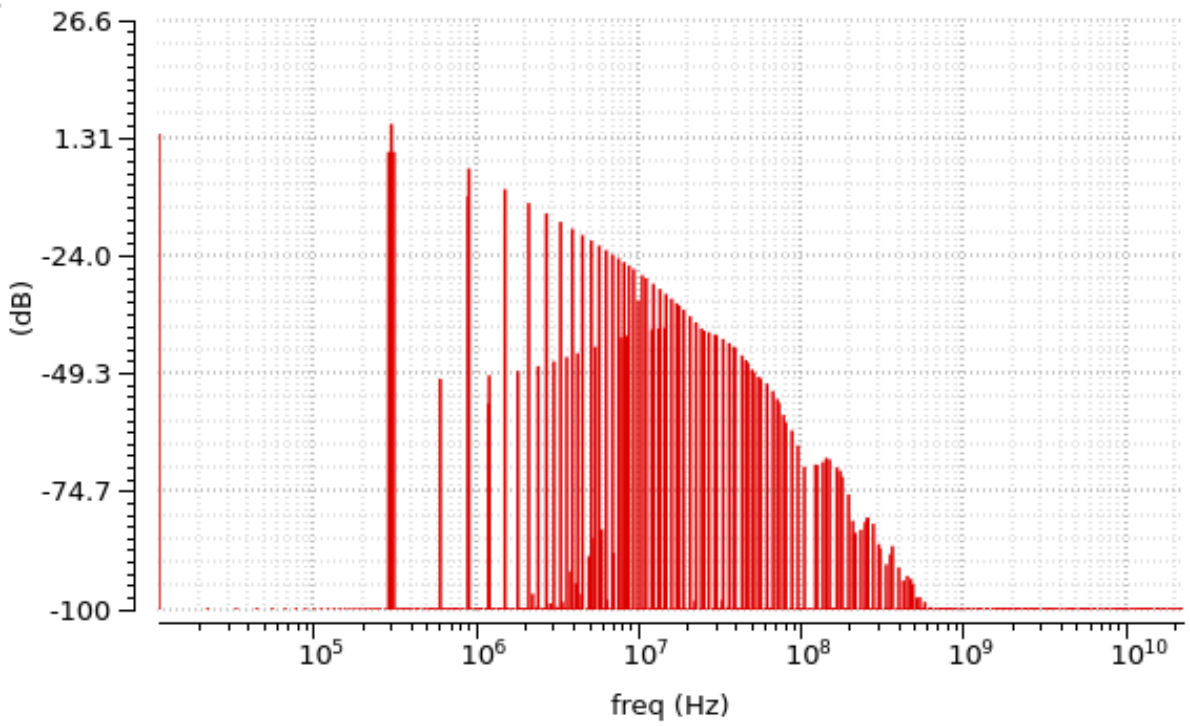


Figure 3.41 – The EMI of OTA-based gate driver

The time-domain improvements are reflected in the EMI results. The spectral plots of the drain voltage show that the OTA suppresses the high-frequency components associated with switching edges. The peaks are strongly attenuated, and the overall high-frequency envelope is significantly lower. This reduction is achieved at the cost of increased switching loss, since slowing and smoothing the transition increases the energy dissipated per transition. The improved EMI in combination with the reduced sensitivity to variations make the OTA-based driver an attractive option in applications where electromagnetic

compatibility is a primary constraint and some amount of switching losses is acceptable.

CHAPTER 4 COMPARATIVE ANALYSIS AND DISCUSSION

4.1 EMI Performance Comparison

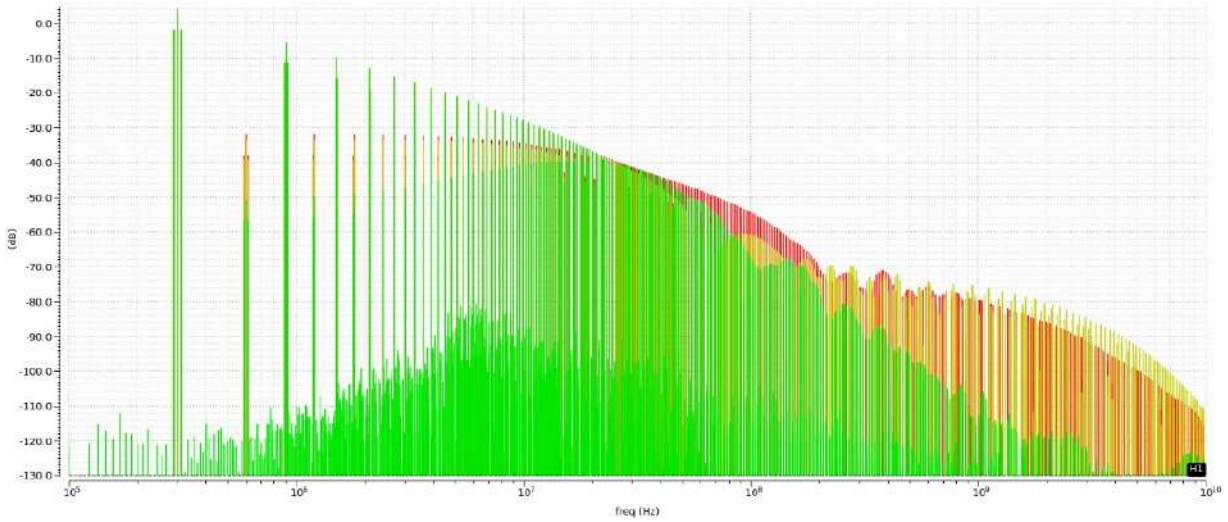


Figure 4.1 – The EMI of PP (red), SOA (yellow) and OTA (green)

The electromagnetic interference performance of the three gate-driver topologies was evaluated by comparing the frequency spectra of the drain voltage under identical operating conditions using the boost converter circuit load. The magnitude spectra are plotted side-by-side for direct comparison

4.1.1 Push-pull gate driver

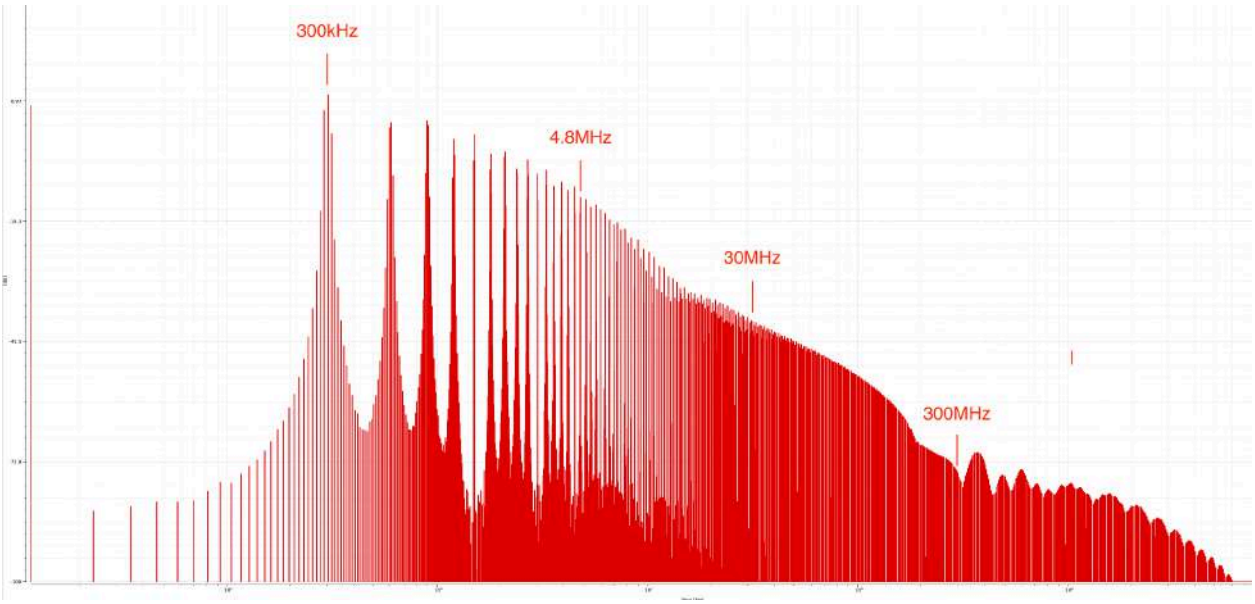


Figure 4.2 – EMI of push-pull gate driver

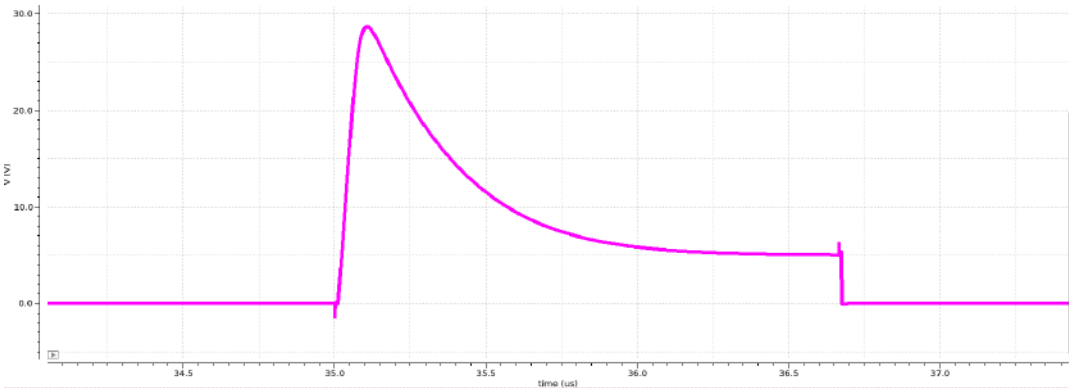


Figure 4.3 – Vds of power MOSFET of push-pull gate driver

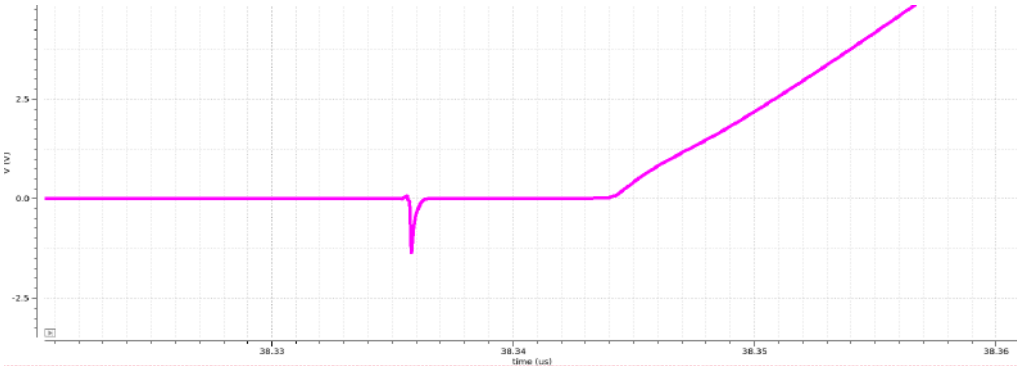


Figure 4.4 – Zoomed-in voltage spike on rising edge of Vds

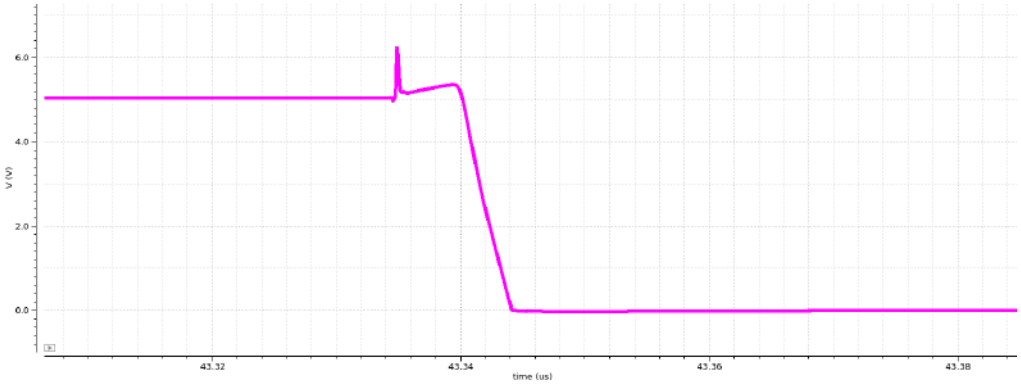


Figure 4.5 – Zoomed-in voltage spike on falling edge of Vds

The voltage spikes on Vds of power MOSFET for the conventional push-pull driver result in the expected characteristics of a hard-switched converter. Figure 4.2 shows the magnitude of the fundamental switching harmonics remains high, with a broad pedestal of noise energy extending well into the Very High Frequency (VHF) region of 30 - 300 Mhz. Resonant peaks correspond to the natural ringing frequency of the power loop parasitic inductance and the MOSFET

output capacitance. This unconstrained dv/dt and underdamped ringing inject significant high-frequency content that would likely exceed standard EMC limits (e.g., CISPR 25 - 150 kHz to 5,925 GHz) without bulky external filtering[20].

4.1.2 Segmented gate driver



Figure 4.6 – The EMI of SOA

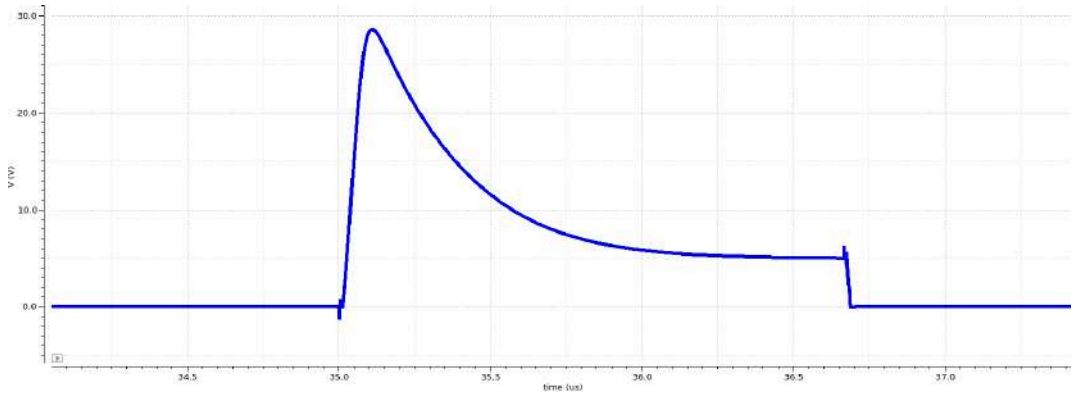


Figure 4.7 – Vds of power MOSFET of SOA gate driver

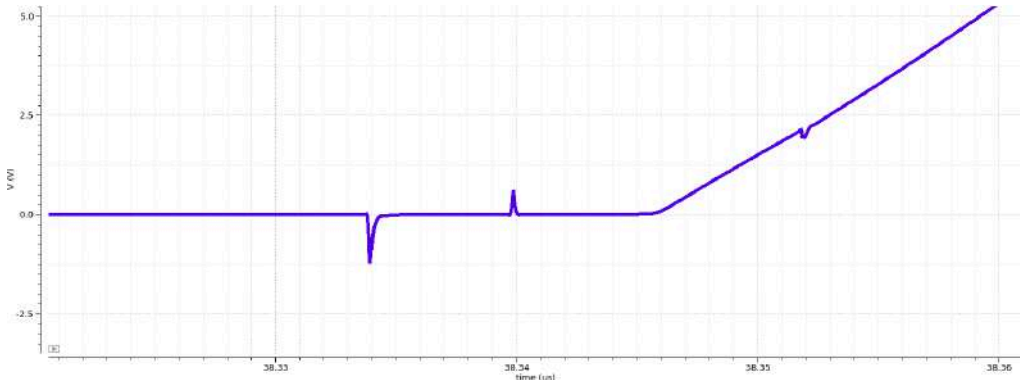


Figure 4.8 – Zoomed-in voltage spikes on rising edge of Vds

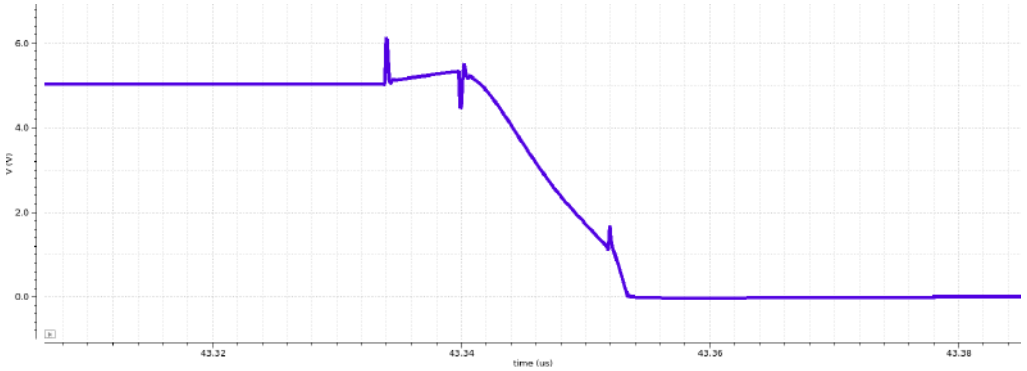


Figure 4.9 – Zoomed-in voltage spikes on falling edge of Vds

The segmented digital driver demonstrates a slight improvement over the baseline. The high-frequency noise envelope decays more rapidly. The resonant peaks associated with the power stage parasitics are slightly diminished. The spectrum retains visible artifacts of the underlying LC dynamics, energy remains around the ringing frequency, and the attenuation at higher harmonics is not uniform. The segmentation slightly redistributes the noise energy but, because of its discrete nature, does not fully suppress the resonant peaks.

4.1.3 OTA-based driver

The comparison between a classic folded cascode and ENRFC is solely for illustrative purposes. The classic folded cascode shows incredible EMI improvement at the whole spectrum and its Vds shows the smoothest curve among all. The reasons why this topology shows such results will become evident after the efficiency and Vgs waveform comparison later in this chapter.

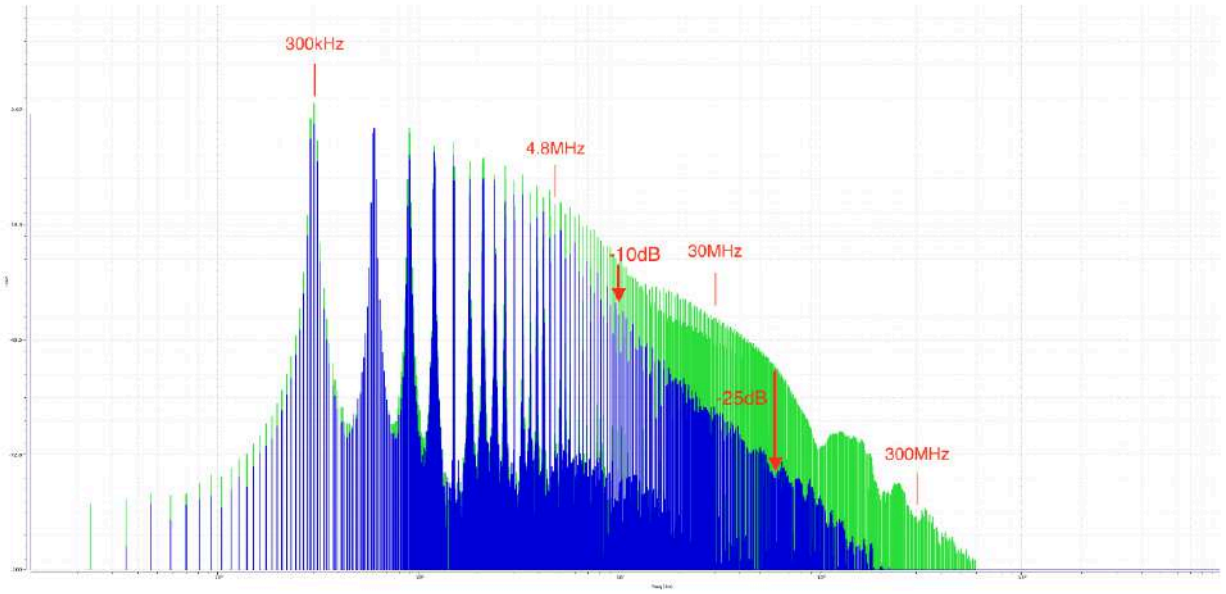


Figure 4.10 – The EMI comparison of classic folded cascode OTA (blue) and ENRFC (green)

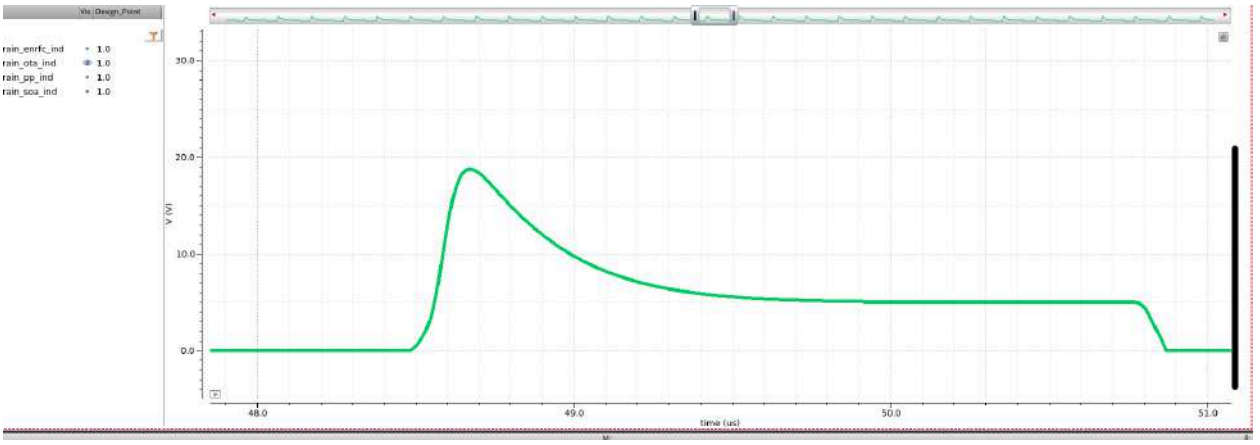


Figure 4.11 – Vds of power MOSFET of classic folded cascode OTA-based gate driver

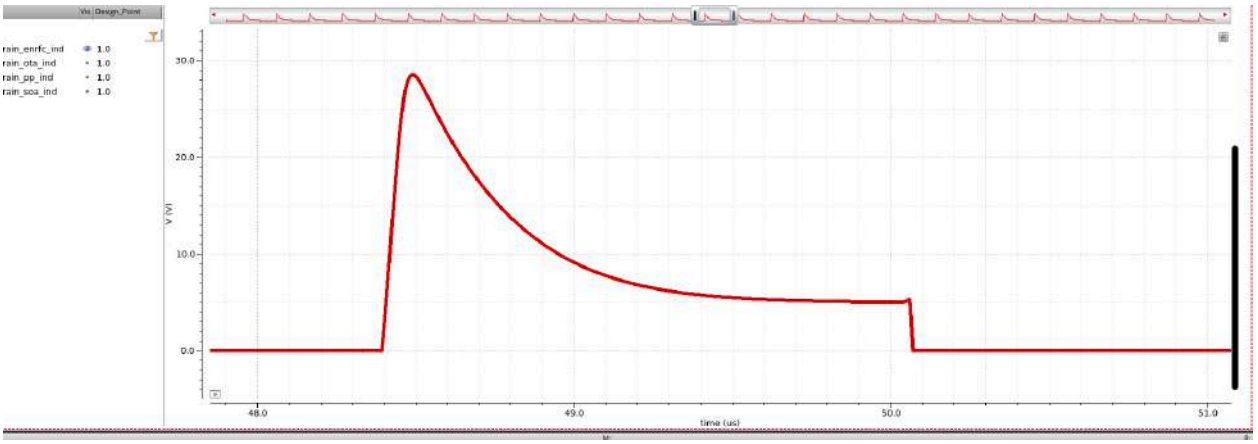


Figure 4.12 – Vds of power MOSFET of ENRFC OTA-based gate driver

For the same effective switching frequency, the magnitudes of the harmonics are reduced starting from around 80Mhz and until the end of frequency range showing a much faster roll-off. The resonant peaks caused by the parasitic LC tank are strongly suppressed. This behavior confirms that the continuous-time feedback loop successfully forces Vgs to track the hyperbolic curve, preventing the slope changes that excite high-frequency parasitics.

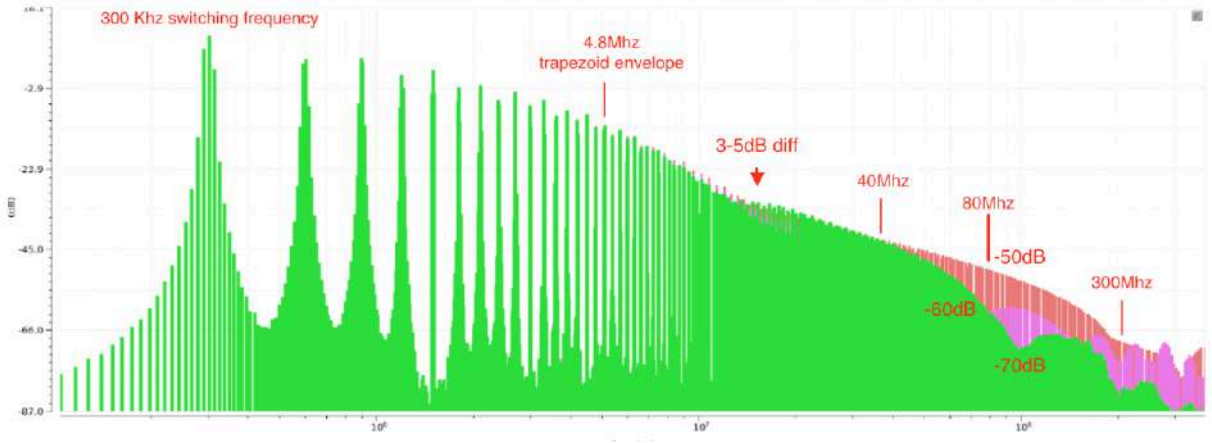


Figure 4.13 – EMI of push-pull (red), SOA (pink) and ENRFC (green)

The comparison at specific frequencies of interest highlights the performance gap. The spectra below 5MHz match as all three drivers produce the same drain rise time around 60 ns and the trapezoid envelope is almost identical. From 5 to 80 MHz there are small differences around 3-5 dB that come from different transition shapes even with equal 10–90% rise time. Above 80 MHz the

SOA drain waveform shows short spikes of < 20 ns that inject VHF content and excite parasitic resonances. The OTA effectively dampens these spikes, showing a large high-frequency EMI reduction. The most relevant on-board receivers in 30 to 300 MHz spectrum are FM (87.5 - 108 MHz) and DAB in some countries (174 - 240 MHz), therefore emissions in this band are strongly correlated with audible radio noise.

4.2 Switching Efficiency versus EMI Performance

Table 4.1 – Efficiency calculation results

Topology	**Gate driver losses P1 (u)**	**Push-Pull losses P2 (u)**	**Switching losses P3 (u)**	**Pload (u)**	**Efficiency %**
Push-pull	0.0028	0.4626	5.401	41.35	87.58
SOA (P1 + P2)	-	0.5442	5.407	41.26	87.39
Folded OTA	0.0065	8.638	3.668	23.75	65.86
ENRFC	0.0674	0.9868	5.392	41.06	86.43

This table presents the comparison of the trade-off between electromagnetic interference and switching efficiency for the gate-driver topologies. The direct extraction of pure switching losses from simulation is non-trivial since conduction losses, leakage, and driver consumption are all intertwined. For this reason, system efficiency is the most easily obtained yet informative metric that can be used as a counter-metric to EMI. The efficiency is defined as:

$$\eta = \frac{P_{out}}{P_{in}} \tag{4.1}$$

and is evaluated for the same load and supply voltage while varying the gate-drive settings. Any reduction in η observed under these conditions is therefore dominated by increased switching and driver losses, and can be interpreted as the price of achieving a given level of EMI reduction.

The classic folded cascode is added to comparison as it is important to show at what price comes its EMI improvement. The push-pull driver sets the upper bound with an efficiency of approximately 87%. This represents the "hard-switching" limit where switching overlap losses are minimized but EMI generation is maximal.

The segmented driver shows approximately the same calculated efficiency of 87%. The tiny difference represents the energy cost of stepping the gate voltage to smooth the transition. This topology slightly lowers the EMI floor, and slightly lowers the efficiency.

The ENRFC-based driver shows slightly lower efficiency at approximately 85%. This is caused by the static power consumption of the OTA circuit and the extended time required to replicate the smooth hyperbolic curve. This step requires almost twice the energy compared to SOA or push-pull. This confirms that the EMI improvement comes at a price, making it suitable specifically for applications where EMI compliance is more important than efficiency.

The classic cascode shows the lowest efficiency of about 65%. While showing lowest load and switching losses, this topology shows incredibly high push-pull (output stage) losses, almost 8 times higher than ENRFC and almost 16 times higher than SOA.

The comparison of gate and drain voltages sum up the findings. Push-pull and SOA showing spikes and overshoots while ENRFC shows a desired hyperbolic

curve. The plots of classical folded cascode confirm that this topology is unable to charge and discharge the gate fast enough and high enough because of its limited slew rate.



Figure 4.14 – Vgs comparison



Figure 4.15 – Vgs rising edge comparison



Figure 4.16 – Vgs falling edge comparison



Figure 4.17 – Vds comparison

4.3 Discussion of Complexity and Feasibility

Beyond the performance metrics of EMI and efficiency, the three gate-driver topologies differ significantly in implementation complexity and practical feasibility. From a physical design perspective, each topology presents distinct layout challenges, although a precise comparison requires post-layout extraction

The Push-Pull Driver represents the simplest solution. Its core consists of a single CMOS inverter or a small chain of inverters sized to deliver the required gate current. Transistor count, biasing complexity, and verification effort are

minimal so the circuit is straightforward to implement. This is why the push-pull driver remains the default choice for cost-sensitive systems where EMI is addressed via external filtering. As for the layout, the push-pull requires a compact, symmetric placement near to the power MOSFET, minimizing gate-loop inductance.

The segmented driver occupies an intermediate position. While the output stage is still built from conventional inverter legs, the replication of these legs significantly increases the component count. For the 4-bit segmentation considered in this work, the number of output transistors increases by a factor of four relative to a single-leg driver. Furthermore, the inclusion of the digital control block (the edge-detection and phase-generation logic) adds an extra layer of digital complexity. Despite the transistor count, the design remains conceptually simple. There is no high-gain feedback loop and stability concerns are limited to digital timing and output ringing. It aligns well with mixed-signal flows and allows integration into microcontroller-driven power stages. As for the layout, the challenge is primarily routing and matching. The layout requires the precise replication of parallel legs to ensure identical current sharing. Additionally, the routing of the multiple control lines creates local congestion, requiring careful shielding to prevent digital switching noise from coupling into the gate output.

The OTA-based driver with Vgs feedback is the most demanding in terms of circuit design. In addition to the output buffer, it requires a high-performance operational transconductance amplifier, a precise reference-shaping filter, and a feedback network. When the nonlinear current-recycling OTA is used, the transistor count exceeds the segmented driver circuit due to the complex adaptive biasing and current mirror networks. Ensuring loop stability across process, voltage, and temperature (PVT) corners while preserving the slew-rate enhancement presents a difficult analog verification task. Unlike the robust digital logic of the segmented driver, the OTA is sensitive to device mismatch and internal bias drifts. The main layout challenge is noise isolation. The layout must place the

OTA inputs next to a switching buffer. The input stage requires differential pair matching and guard-ring isolation to reject the massive dv/dt and di/dt noise generated by the nearby power device. It is important to place the OTA close enough to the gate for signal integrity and far enough to preserve analog performance. This represents a non-trivial floorplanning trade-off.

These differences suggest distinct target domains for each topology:

- **Push-Pull:** Best for cost-driven, high-efficiency applications where standard EMI compliance is sufficient.
- **Segmented:** Best for applications requiring configurable slew-rate control without the risk and complexity of a full analog feedback loop.
- **OTA-Based:** Best for high-performance, EMI-critical systems (e.g., automotive or aerospace) where the precise control of the switching waveform justifies the increased silicon area and design complexity.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

5.1 Summary of Work

The primary goal of this thesis was to investigate if the shape of Vgs could be modified to reduce the electromagnetic interference to a level where the overall efficiency of the system

$$\eta = P_{\text{out}}/P_{\text{in}} \tag{5.1}$$

remains at an acceptable level. Three topologies were simulated and analyzed starting from a conventional push-pull driver, moving through a segmented state-of-the-art digital driver, and finishing with an OTA-based driver with analog feedback and a pre-shaped reference curve for Vgs.

The first reviewed topology was the basic CMOS push-pull gate driver with asymmetric sizing which served as the baseline for comparison in both complexity and performance. The Vds shows rapid changes during the Miller plateau and the parasitic inductances in the power stage are excited by underdamped switching event. High-frequency components and resonance-related peaks are visible in the spectral analysis of the Vds node of the power MOSFET. Despite its downsides, this topology has the easiest design complexity and best switching efficiency.

The second reviewed topology was the state of the art segmented digitally controlled gate driver. The large push-pull stage was replaced with four identical legs with pull up/down sides. For the purpose of simulation, this driver is controlled by the Verilog-A block that divides each PWM edge into four time windows and enables subsets of legs based on the 4-bit code pattern. These separate rise and fall time patterns allowed to shape the instantaneous gate-drive strength. The pattern 4 - 1 - 1 - 4 was used to limit the peak dVgs/dt. The Vgs waveform though being continuous exhibited clear spikes when the leg count changed. This topology generally allowed for slightly lower overshoot and ringing compared to the basic driver and showed slight improvements to the EMI spectrum.

The final reviewed topology was the OTA-based gate driver that uses local negative feedback from the gate of power MOSFET. At first, the target Vgs voltage waveform was defined in the time domain as a hyperbolic-like transition with a 10-90 % rise time of about 40 ns. The waveform's poles and zeros were identified in MATLAB and then approximated by a high-order LTI filter, with later implementation in Verilog-A as the PWM_hyperbolic block. As a result, the filter converts the PWM signal input into a continuous reference waveform for Vgs. The OTA's function is to observe the difference between the filtered signal and the actual Vgs of the power MOSFET. Two OTA topologies were tested: a classic folded cascode and a nonlinear current-recycling folded cascode with enhanced gain-bandwidth and slew-rate characteristics. The results showed that both tested topologies are capable of forcing Vgs to follow the reference pattern, however, only enhanced folded cascode topology can do it within the specified 40ns. The Vds transitions became free of sharp edges and exhibited only small, heavily damped residual oscillations. As for the EMI comparison, this topology showed the lowest spectral emissions among all three drivers with a rapid decay of the high-frequency envelope and significant attenuation of resonance-related peaks. The price for lowering EMI is increased power losses caused by smoothed switching transitions and the lowest efficiency. The OTA-based architecture shows the upper bound of what can be achieved with analog feedback in terms of EMI performance. It provides a technical reference and a design benchmark for future gate-driver improvements.

5.2 Key Findings

The results of this work demonstrates that shaping of the gate-source voltage is an effective way of controlling electromagnetic interference in hard-switched power stages. By spreading the effective drive strength over several time windows and reducing the instantaneous gate current during the Miller plateau, it is possible to suppress voltage overshoots. The switching behavior of the power MOSFET is not defined by the device alone, but can be modified by the gate-control strategy

The OTA based topology with feedback taken from Vgs of power MOSFET and a hyperbolic reference achieves a greater level of control. If high performance OTA topology is used, the feedback forces the gate voltage to follow a smooth waveform which shows Vds transitions with minimal overshoot and heavily damped residual oscillations. This produces the lowest EMI levels among the compared topologies, with strong suppression of both narrowband resonant peaks and broadband high-frequency content. The EMI improvement however comes at a cost of reduction in system efficiency.

- The push-pull topology is the most efficient but also the noisiest.
- The segmented driver shows moderate EMI reduction with relatively small efficiency loss.
- The OTA-based driver shows greatest EMI suppression at the cost of a steeper decline in efficiency and higher implementation complexity.

5.3 Future Work

The presented results are based on simulations with behavioral models for control blocks, partially idealized components and idealized assumptions regarding packaging parasitics without corner simulations. With this being stated, the results do not present a complete manufacturable solution but rather demonstrate the fundamental principle and potential of OTA-based gate shaping. The proposed lines of work may help bridge the gap between concept and real world implementation.

- **Stability analysis.** The OTA closed-loop stability was evaluated for two Vcm points. To get the full picture of the limitations of the presented topology, the stability should be verified across additional operating conditions, including Vcm sweep over the full input range, under different load conditions, different output operating points/duty-cycle regions. Additionally, PVT corners analysis has to be conducted to ensure sufficient phase margin in all modes.

- **On-Chip Reference Generation (DAC Design).** Currently, a Verilog-A block with MATLAB-derived coefficients generates the control signal for the OTA. The first improvement that can be proposed is to generate this signal with a dedicated on-chip Digital-to-Analog Converter (DAC). This gives an opportunity to dynamically adjust the rise/fall time, amplitude, offset enable continuous or discontinuous conduction mode etc. Future work may investigate the architectures suitable for this job (e.g. current-steering or capacitive), the impact of quantization glitches on the tracking loop, required resolution to prevent staircase noise from coupling to the gate. Such an improvement may transform the fixed design with a virtual control block into a truly digitally programmable gate-control system.
- **Layout and Post-Layout Simulation.** Since the results presented here rely on idealized representations of loop inductance; the real device will show the distributed parasitics of the metal interconnects and vias that will affect both the stability of the OTA loop and the EMI performance. The future work must focus on advanced layout techniques like differential shielding, guard ringing, and symmetrical floorplanning. This should be followed by parasitic extraction to verify that the desired gate waveform shaping remains the same in a real environment.
- **Fabrication and Experimental Verification.** Another step is the fabrication of the prototype to confirm the simulation results on a real world testbench using specialized equipment. Laboratory characterization using double-pulse testing (DPT) would help measure the switching energy, voltage overshoot, and EMI. These measurements may expose practical effects not captured in simulation, including ringing caused by packaging, process variation, and the long-term drift of bias conditions. Showing the difference between simulation and silicon measurements is an important step for advancing from a research to a manufacturable solution.

- **Technology Selection and Migration.** The choice of semiconductor technology is an important step that requires careful research. This work used the IHP SG13G2 130nm BiCMOS Open Source process. This technology may be a great fit for the mixed-signal RF research, it is not optimized for high voltage power applications so High-Voltage CMOS or BCD (Bipolar-CMOS-DMOS) technologies would be more appropriate as they offer elevated voltages, automotive temperature ranges, isolated LDMOS devices and integrated high-side level shifters. Migrating the design to another technology would likely alter the trade-offs in terms of device speed, breakdown voltage and parasitic capacitance so it will require some rework and optimization. However, a comparison of the proposed architectures in a more suitable process would provide valuable insight into the scalability of the OTA-based approach for industrial and automotive applications.

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